# Product Change Notice

(PCN tracking number : CST-R2-AD121 Rev.1.0)

February 17, 2017

**To:** Valued RENESAS Customer,

**Renesas Product Summary:** Standard SRAM (TSOP, FBGA, µTSOP and SOJ) products.

**Change Description:**

**Applicable products**

- Part of 32Mb/64Mb LPSRAM products
- Part of 4Mb asynchronous fast SRAM products (= SOJ products)

**Items of change** (They are different for each product. Please see page 3 to 8.)

- Site change of Final-test process
- Site change of assembly process and the change of assembly materials
- Product integration from lower-grade "-5SR, -7SI, -7SR" products to upper-compatible "-5SI" products
- Packing specification

**Reason for Change:** Site change due to obsolescence of manufacturing equipment, and for long-time, stable supply by improvement of mass production efficiency through part name unification.

**Identification:** Identifiable by RENESAS internal code, printed on the shipping label, and also identifiable by the laser-marking on the package's surface for the products of part name unification.

**Anticipated Impact:**

- Packing specification is changed accompanied with the site change of Final-test process for all of the products included in this notification.
- Only regarding the 32Mb 48pin-TSOP(I) product (R1LV3216RSA), Moisture Sensitivity Level is changed from MSL2 to MSL3 accompanied with a change of lead-frame material (42-Alloy to Cu).
- Electrical characteristics of "-5SI" product is completely upper-compatible with "-5SR, -7SI, -7SR" products.

**Date of Change:** From July 2017, onward

**Schedule:**

- Regarding the EOL of 32Mb/64Mb "-5SR, -7SI, -7SR" products,
  EOL Announcement: June, 2017
  Commercial samples of unified "-5SI" product: From March, 2017.
- Regarding the site change of Back-end process (excluding EOL products),
  Mass production of the post-change products from July 2017, in order of preparations.

**Supplemental Information:** Please see the page 3 to 8 and the attachments (Appendix for CST-R2-AD121).

**Contact:** General Purpose Analog and Power Solution Department 3,
General Purpose Analog and Power Business Division,
2nd Solution Business Unit

**Internal Reference:**

**Attachments:** Appendix for CST-R2-AD121

In case of any questions, please contact your Renesas sales representative.

**Customer Response** (to be returned by email or mail)

| | |
|---|---|
| ☐ Acknowledge | Company: _____ |
| ☐ Acceptable | Name & Position: _____ |
| ☐ Unacceptable (pls. comment) | Email: _____ |
| ☐ Not applicable | Phone: _____ |

Note: Acknowledgement must be received by Renesas within 30 days of delivery of the PCN or Renesas will consider the change as approved. If timely acknowledgement is provided by Customer, then Customer shall have 90 days from the date of receipt of this PCN in which to make any objections to the PCN. If Customer fails to make objections to this PCN within 90 days of the receipt of the PCN then Renesas will consider the PCN changes as approved. If customer cannot accept the PCN then customer must provide Renesas with a last time buy demand and purchase order.

**Comments**

| |
|---|
| |

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Signature of customer

## 1. Background of Change

Renesas announces 2 types of Product Changes on Standard SRAM (TSOP, FBGA, µTSOP and SOJ) products.

One is applied to 32Mb/64Mb LPSRAM which include a site change of Back-end process (assembly and/or final-test) and product integration by EOL of "-5SR, -7SI, -7SR" products and by part name unification to the upper compatible "-5SI" products. The site change is due to obsolescence of current manufacturing equipment and the unification is for the purpose of long-time, stable supply by improvement of mass production efficiency.

The other is applied to 4Mb asynchronous fast SRAM which includes a site change of Final-test process for SOJ product. This is also due to obsolescence of current manufacturing equipment.

We greatly appreciate your kind understanding and early approval for this notification.

## 2. Details of Change

■ Regarding the applicable part names of this PCN, please refer to "7. Product list" on page 8.
The details of change are categorized into three as shown below in (1), (2), (3).

### (1) Orderable Part Name: R1LV3216RSA-5SR, -7SI, -7SR#B0/#S0

(a) "Access and Temperature grades" of "-5SR, -7SI, -7SR" in 32Mb 48pin-TSOP(I) products are put to EOL, and part names of the products are unified to "-5SI".

(b) In accordance with product integration by EOL of "-5SR, -7SI, -7SR" products and part name unification to "-5SI" products, there are changes in Back-end process as shown in the table below.

| Item | | | Before product integration by EOL (R1LV3216RSA-5SR, -7SI, -7SR #B0/#S0) | After part name unification (R1LV3216RSA-5SI #B1/#S1) |
|---|---|---|---|---|
| **Assembly** | Company | | Renesas Semiconductor Beijing | Amkor Technology Malaysia |
| | Country | | China | Malaysia |
| | Material | Lead frame | 42Alloy | Cu |
| | | Lead plating | Sn-Cu | Sn |
| | Package marking: Country of origin | | CHINA | MALAYSIA |
| **Moisture Sensitivity Level** | | | MSL 2 | MSL 3 |
| **Final-test** | Company | | Renesas Semiconductor Beijing | Powertech Technology Inc. |
| | Country | | China | Taiwan |
| **Packing specification** | Tray packing | | Current specification | New specification |
| | | | ・Tray type name, PKG seat position in tray pocket, Number of trays(Max.), and Inner-box size are changed. For more details, see the appendix. | |
| | Tape & Reel packing | | Current specification | New specification |
| | | | ・Type name of Embossed tape and Inner-box size are changed. For more details, see the appendix. | |

(c) Regarding these changes,

- Electrical characteristics (DC/AC) of unified "-5SI" product are completely upper-compatible with "-5SR, -7SI, -7SR" products. For more details, please see the comparison tables on the appendix.
- "Access and Temperature grades" which is laser-marked on package's surface, is changed from "-5SR, -7SI, -7SR" to "-5SI."
- Although assembly materials are changed, package outline and pin configuration are equivalent to those of pre-change products which keep board-level package reliability.
- There are no changes in the site of Front-end (Wafer) process or revision of photomasks.
- There are no changes in Reliability and quality level.
- The last characters of orderable part name are changed from #B0/#S0 to #B1/#S1, accompanied with the change of assembly site and materials.

(2) **Orderable Part Name: R1WV6416RSA-5SR, -7SI, -7SR#B0/#S0**
**R1WV6416RBG-5SR, -7SI, -7SR#B0/#S0**
**R1LV3216RSD-5SR, -7SI, -7SR#B0/#S0**
**R1WV6416RSD-5SR, -7SI, -7SR#B0/#S0**

(a) "Access and Temperature grades" of "-5SR, -7SI, -7SR" in above 32Mb/64Mb LPSRAM products are put to EOL, and part names of the products are unified to "-5SI".
(Regarding the part names after unification, please refer to "7. Product list" on page 8.)

(b) In accordance with product integration by EOL of "-5SR, -7SI, -7SR" products and part name unification to "-5SI" products, there are changes in Final-test site and packing specification as shown in the table below.

<table>
<tr><th colspan="2">Item</th><th>Before product integration by EOL<br>(-5SR, -7SI, -7SR#B0/#S0)</th><th>After part name unification<br>(-5SI#B0/#S0)</th></tr>
<tr><td rowspan="2">Final-test</td><td>Company</td><td>Renesas Semiconductor Beijing</td><td>Powertech Technology Inc.</td></tr>
<tr><td>Country</td><td>China</td><td>Taiwan</td></tr>
<tr><td rowspan="4">Packing specification</td><td rowspan="2">Tray packing</td><td>Current specification</td><td>New specification</td></tr>
<tr><td colspan="2">・Regarding R1WV6416RSA,<br>Tray type name, PKG seat position in tray pocket, Number of trays(Max.) and Inner-box size are changed. For more details, see the appendix.<br>・Regarding R1WV6416RBG, R1LV3216RSD and R1WV6416RSD,<br>Laying direction of ICs on a tray, Number of trays(Max.) and Inner-box size are changed. For more details, see the appendix.</td></tr>
<tr><td rowspan="2">Tape & Reel packing</td><td>Current specification</td><td>New specification</td></tr>
<tr><td colspan="2">・Regarding R1WV6416RSA,<br>Type name of Embossed tape and Inner-box size are changed. For more details, see the appendix.<br>・Regarding R1WV6416RBG, R1LV3216RSD and R1WV6416RSD,<br>Inner-box size is changed. For more details, see the appendix.</td></tr>
</table>

(c) Regarding these changes,

- Electrical characteristics (DC/AC) of unified "-5SI" product are completely upper-compatible with "-5SR, -7SI, -7SR" products. For more details, please see the comparison tables on the appendix.
- "Access and Temperature grades" which is laser-marked on package's surface, is changed from "-5SR, -7SI, -7SR" to "-5SI."
- There are no changes in assembly site or assembly materials.
  (The changes in assembly site and assembly materials are only applicable to 32Mb 48pin-TSOP(I) products: R1LV3216RSA on page 4.)
- There are no changes in the site of Front-end (Wafer) process or revision of photomasks.
- There are no changes in Reliability and quality level.

(3) **Orderable Part Name: R1WV6416RSA-5SI#B0/#S0**
**R1RP0408DGE-0PI, -0PR, -2LR, -2PI, -2PR#B0**
**R1RW0408DGE-0PI, -0PR, -2LR, -2PI, -2PR#B0**
**R1RP0416DGE-0PR, -2LR, -2PI, -2PR, -2SR, -2UR, -2VR#B0**
**R1RW0416DGE-0PR, -2LR, -2PI, -2PR, -2SR, -2UR#B0**

(a) Regarding these products, there are changes in Final-test site and packing specification as shown in the table below.

| Item | | Pre Change | Post Change |
|---|---|---|---|
| **Final-test** | Company | Renesas Semiconductor Beijing | Powertech Technology Inc. |
| | Country | China | Taiwan |
| **Packing specification** | Tray packing | Current specification | New specification |
| | | ・Tray type name, PKG seat position in tray pocket, Number of trays(Max.) and Inner-box size are changed. For more details, see the appendix. | |
| | Tape & Reel packing | Current specification | New specification |
| | | ・Type name of Embossed tape and Inner-box size are changed. For more details, see the appendix. | |
| | Magazine packing (Tube packing) | Current specification | New specification |
| | | ・Inner-box size is changed. For more details, see the appendix. | |

(b) Regarding these changes,

- There are no changes in assembly site or assembly materials.
  (The changes in assembly site and assembly materials are only applicable to 32Mb 48pin-TSOP(I) products: R1LV3216RSA on page 4.)
- There are no changes in the site of Front-end (Wafer) process or revision of photomasks.
- There are no changes in Reliability and quality level.
- There are no changes in Electrical characteristics (DC/AC).
- Orderable part names are not changed.

## 3. Release Support and Milestones

| | |
|---|---|
| **Sample submission** | (1) Regarding the site change of final-test process,<br>we are not planning to supply samples.<br>(2) Regarding the EOL of "-5SR, -7SI, -7SR" products,<br>we will supply commercial samples of unified "-5SI" from March, 2017. |
| **Renesas report** | (1) Regarding the site change of final-test process,<br>we are not planning to submit the reliability report.<br>(2) Regarding the EOL of "-5SR, -7SI, -7SR" products,<br>we will submit the reliability report of unified "-5SI" from March, 2017. |

## 4. Identification

(1) Identifiable by RENESAS internal code, printed on the shipping label

(2) Also, identifiable by the laser-marking on the package's surface for the products of part name unification.
For more information, please see the attachments (Appendix for CST-R2-AD121).

## 5. Schedule

(1) Regarding the EOL of "-5SR, -7SI, -7SR" products,
EOL Announcement: June, 2017
Commercial samples of unified "-5SI" product: From March, 2017

(2) Regarding the site change of Back-end process (excluding EOL products),
Mass production of the post-change products from July 2017, in order of preparations.

## 6. Supplemental Information

Please see the attachments (Appendix for CST-R2-AD121).

## 7. Product list

| Package type | Product Type (Memory Cap., Supply Voltage) | Orderable part name | |
|---|---|---|---|
| | | Pre Change | Post Change |
| 48pin-TSOP(I) | 32Mb 3V | R1LV3216RSA-5SR, -7SI, -7SR#B0 | R1LV3216RSA-5SI#B1 |
| | | R1LV3216RSA-5SR, -7SI, -7SR#S0 | R1LV3216RSA-5SI#S1 |
| | 64Mb 3V | R1WV6416RSA-5SI#B0 | ← |
| | | R1WV6416RSA-5SI#S0 | ← |
| | | R1WV6416RSA-5SR, -7SI, -7SR#B0 | R1WV6416RSA-5SI#B0 |
| | | R1WV6416RSA-5SR, -7SI, -7SR#S0 | R1WV6416RSA-5SI#S0 |
| 48ball-FBGA | 64Mb 3V | R1WV6416RBG-5SR, -7SI, -7SR#B0 | R1WV6416RBG-5SI#B0 |
| | | R1WV6416RBG-5SR, -7SI, -7SR#S0 | R1WV6416RBG-5SI#S0 |
| 52pin-µTSOP | 32Mb 3V | R1LV3216RSD-5SR, -7SI, -7SR#B0 | R1LV3216RSD-5SI#B0 |
| | | R1LV3216RSD-5SR, -7SI, -7SR#S0 | R1LV3216RSD-5SI#S0 |
| | 64Mb 3V | R1WV6416RSD-5SR, -7SI, -7SR#B0 | R1WV6416RSD-5SI#B0 |
| | | R1WV6416RSD-5SR, -7SI, -7SR#S0 | R1WV6416RSD-5SI#S0 |
| 36pin-SOJ | 4Mb Fast 5V | R1RP0408DGE-0PI, -0PR, -2LR, -2PI, 2PR#B0 | ← |
| | 4Mb Fast 3V | R1RW0408DGE-0PI, -0PR, -2LR, -2PI, 2PR#B0 | ← |
| 44pin-SOJ | 4Mb Fast 5V | R1RP0416DGE-0PR, -2LR, -2PI, 2PR, -2SR, -2UR, -2VR#B0 | ← |
| | 4Mb Fast 3V | R1RW0416DGE-0PR, -2LR, -2PI, 2PR, -2SR, -2UR#B0 | ← |

・ Regarding unlisted orderable part names of pre-change products here in 32Mb/64Mb line-up, R1LV3216RSA-5SI#B0/#S0 is already announced in August, 2016 (document No. CST-R2-AJ094), as a site change of Back-end process (assembly and final-test) including a change of assembly materials. RMWV3216AGBG-5S2#AC0/#KC0, R1WV6416RBG-5SI#B0/#S0, R1LV3216RSD-5SI#B0/#S0 and R1WV6416RSD-5SI#B0/#S0 are already announced in August, 2016 (document No. CST-R2-AJ095), as a site change of Final-test process.

To: Valued RENESAS customer,

General Purpose Analog and Power Solution Department 3
General Purpose Analog and Power Business Division
2nd Solution Business Unit
Renesas Electronics Corporation

February 17, 2017

# Appendix for CST-R2-AD121
# (Standard SRAM (TSOP, FBGA, µTSOP and SOJ) products)

This appendix states the detailed information of PCN: CST-R2-AD121 (Regarding 32Mb/64Mb LPSRAM, site change of Back-end process (assembly and/or final-test) and product integration by EOL of “-5SR, -7SI, -7SR” products. Regarding 4Mb Asynchronous Fast SRAM, site change of final-test process for SOJ product.).

## Contents

# 1. Product List

(1) 32Mb / 64Mb : 48pin-TSOP(I), 48ball-FBGA, 52pin-μTSOP package

| Package Type | Product Type (Memory Cap., Supply Voltage) | Organi-zation (bit) | Orderable Part Name | | Packing Type | Page No. of Comparison Table |
|---|---|---|---|---|---|---|
| | | | **Pre Change** | **Post Change** | | |
| 48pin-TSOP(I) | 32Mb 3V | x16 | R1LV3216RSA-5SR#B0 | R1LV3216RSA-5SI#B1 | Tray | p.4, p.13, pp.14-15 |
| | | | R1LV3216RSA-7SI#B0 | | | |
| | | | R1LV3216RSA-7SR#B0 | | | |
| | | | R1LV3216RSA-5SR#S0 | R1LV3216RSA-5SI#S1 | Tape & Reel | |
| | | | R1LV3216RSA-7SI#S0 | | | |
| | | | R1LV3216RSA-7SR#S0 | | | |
| | 64Mb 3V | x16 | R1WV6416RSA-5SI#B0 | R1WV6416RSA-5SI#B0 | Tray | p.5, p.13, pp.16-17 |
| | | | R1WV6416RSA-5SR#B0 | | | |
| | | | R1WV6416RSA-7SI#B0 | | | |
| | | | R1WV6416RSA-7SR#B0 | | | |
| | | | R1WV6416RSA-5SI#S0 | R1WV6416RSA-5SI#S0 | Tape & Reel | |
| | | | R1WV6416RSA-5SR#S0 | | | |
| | | | R1WV6416RSA-7SI#S0 | | | |
| | | | R1WV6416RSA-7SR#S0 | | | |
| 48ball-FBGA | 64Mb 3V | x16 | R1WV6416RBG-5SR#B0 | R1WV6416RBG-5SI#B0 | Tray | p.6, p.13, pp.16-17 |
| | | | R1WV6416RBG-7SI#B0 | | | |
| | | | R1WV6416RBG-7SR#B0 | | | |
| | | | R1WV6416RBG-5SR#S0 | R1WV6416RBG-5SI#S0 | Tape & Reel | |
| | | | R1WV6416RBG-7SI#S0 | | | |
| | | | R1WV6416RBG-7SR#S0 | | | |
| 52pin-μTSOP | 32Mb 3V | x16 | R1LV3216RSD-5SR#B0 | R1LV3216RSD-5SI#B0 | Tray | p.7, p.13, pp.14-15 |
| | | | R1LV3216RSD-7SI#B0 | | | |
| | | | R1LV3216RSD-7SR#B0 | | | |
| | | | R1LV3216RSD-5SR#S0 | R1LV3216RSD-5SI#S0 | Tape & Reel | |
| | | | R1LV3216RSD-7SI#S0 | | | |
| | | | R1LV3216RSD-7SR#S0 | | | |
| | 64Mb 3V | x16 | R1WV6416RSD-5SR#B0 | R1WV6416RSD-5SI#B0 | Tray | p.8, p.13, pp.16-17 |
| | | | R1WV6416RSD-7SI#B0 | | | |
| | | | R1WV6416RSD-7SR#B0 | | | |
| | | | R1WV6416RSD-5SR#S0 | R1WV6416RSD-5SI#S0 | Tape & Reel | |
| | | | R1WV6416RSD-7SI#S0 | | | |
| | | | R1WV6416RSD-7SR#S0 | | | |

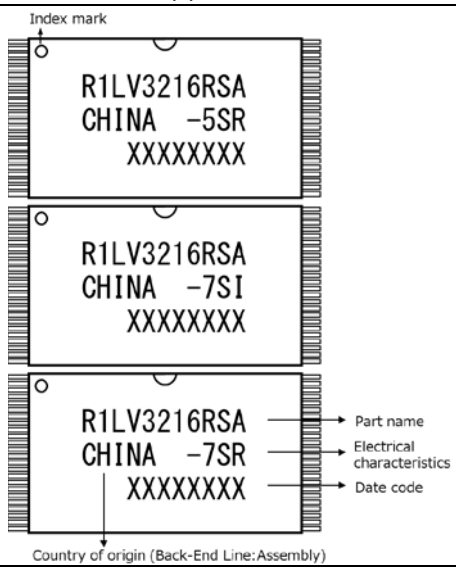
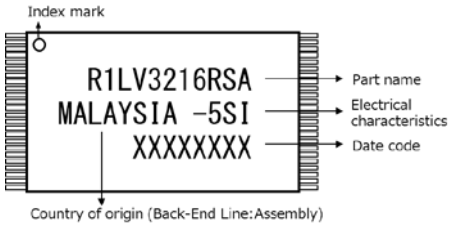
- Regarding unlisted orderable part names of pre-change products here,
  R1LV3216RSA-5SI#B0/#S0 are already announced in August, 2016 (document No. CST-R2-AJ094),
  as a site change of Back-end process (assembly and final-test) including a change of assembly materials.
  R1WV6416RBG-5SI#B0/#S0, R1LV3216RSD-5SI#B0/#S0 and R1WV6416RSD-5SI#B0/#S0 are already announced in August, 2016 (document No. CST-R2-AJ095), as a site change of Final-test process.

(2) 4Mb Fast SRAM：36pin-SOJ, 44pin-SOJ package

| Package Type | Product Type (Memory Cap., Supply Voltage) | Organi-zation (bit) | Orderable Part Name | | Packing Type | Page No. of Comparison Table |
|---|---|---|---|---|---|---|
| | | | **Pre Change** | **Post Change** | | |
| 36pin-SOJ | 4Mb Fast 5V | x8 | R1RP0408DGE-0PI#B0 | ← | Magazine | p.9 |
| | | | R1RP0408DGE-0PR#B0 | ← | | |
| | | | R1RP0408DGE-2LR#B0 | ← | | |
| | | | R1RP0408DGE-2PI#B0 | ← | | |
| | | | R1RP0408DGE-2PR#B0 | ← | | |
| | 4Mb Fast 3V | x8 | R1RW0408DGE-0PI#B0 | ← | Magazine | p.10 |
| | | | R1RW0408DGE-0PR#B0 | ← | | |
| | | | R1RW0408DGE-2LR#B0 | ← | | |
| | | | R1RW0408DGE-2PI#B0 | ← | | |
| | | | R1RW0408DGE-2PR#B0 | ← | | |
| 44pin-SOJ | 4Mb Fast 5V | x16 | R1RP0416DGE-0PR#B0 | ← | Magazine | p.11 |
| | | | R1RP0416DGE-2LR#B0 | ← | | |
| | | | R1RP0416DGE-2PI#B0 | ← | | |
| | | | R1RP0416DGE-2PR#B0 | ← | | |
| | | | R1RP0416DGE-2SR#B0 | ← | | |
| | | | R1RP0416DGE-2UR#B0 | ← | | |
| | | | R1RP0416DGE-2VR#B0 | ← | | |
| | 4Mb Fast 3V | x16 | R1RW0416DGE-0PR#B0 | ← | Magazine | p.12 |
| | | | R1RW0416DGE-2LR#B0 | ← | | |
| | | | R1RW0416DGE-2PI#B0 | ← | | |
| | | | R1RW0416DGE-2PR#B0 | ← | | |
| | | | R1RW0416DGE-2SR#B0 | ← | | |
| | | | R1RW0416DGE-2UR#B0 | ← | | |

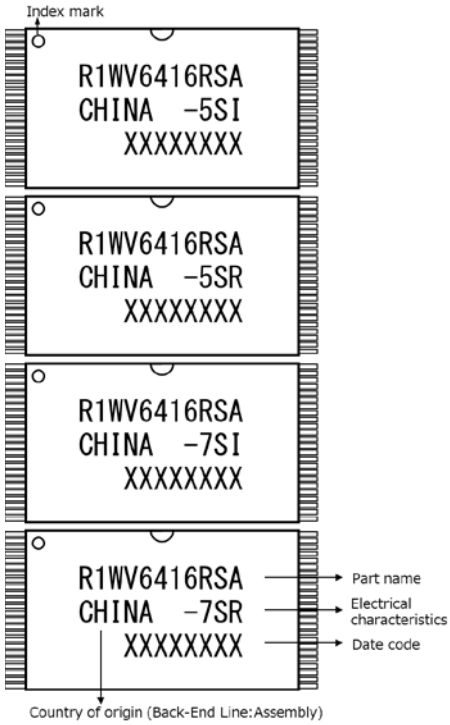
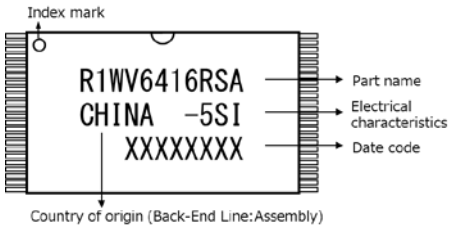
## 2. Comparison table

(1) 48pin-TSOP(I) 32Mb(3V) Part name : R1LV3216RSA

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1LV3216RSA-5SR/-7SI/-7SR#B0 (Tray packing)<br>R1LV3216RSA-5SR/-7SI/-7SR#S0 (Tape & Reel packing) | R1LV3216RSA-5SI#B1 (Tray packing)<br>R1LV3216RSA-5SI#S1 (Tape & Reel packing) |
| Assembly line | | Renesas Semiconductor Beijing (China) | Amkor Technology Malaysia (Malaysia) |
| Country of origin display | | CHINA | MALAYSIA |
| JEITA Package Code | | P-TSOP(1)48-12x18.4-0.50 | P-TSOP(1)48-12x18.4-0.50 |
| Package marking specification | |  |  |
| Assembly Material | Lead frame material | 42Alloy | Cu |
| | Lead plating | Sn-Cu | Sn (pure tin) |
| | Die bonding | Epoxy film | Epoxy paste |
| | Wire bonding | Au | Au |
| | Mold | Epoxy resin (Halogen-included) | Epoxy resin (Halogen-free) |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Tray packing | Packing specification | Current specification | New specification |
| | Tray | JEDEC Tray with Renesas Logo<br>(TSOP I package size: 12mm x 18.4mm) | JEDEC Tray without Renesas Logo<br>(TSOP I package size: 12mm x 18.4mm) |
| | Storage number | 96pcs/tray | 96pcs/tray |
| | Laying direction of ICs on a tray | Direction from the top left position to the down side<br>(when the position of chamfer in tray's corner is bottom left.) | No change |
| | Number of trays (Max.) | 8 trays + 1 tray (cover) | 10 trays + 1 tray (cover) |
| | Inner box size (LxWxH) | 330mm x 152mm x 75mm | 351mm x 175mm x 104mm |
| Tape & Reel packing | Packing specification | Current specification | New specification |
| | Embossed tape | Current specification (type name : TE3216-16P) | New specification (type name : TSOP48-3) |
| | Storage number | 1,000pcs/reel | 1,000pcs/reel |
| | Inner box size (LxWxH) | 347mm x 368mm x 54mm | 362mm x 340mm x 60mm |
| Moisture-proof performance | | MSL 2 | MSL 3 |
| Shipping label | | Current specification | No change in format (Changes in orderable part name, country of origin and MSL display) |

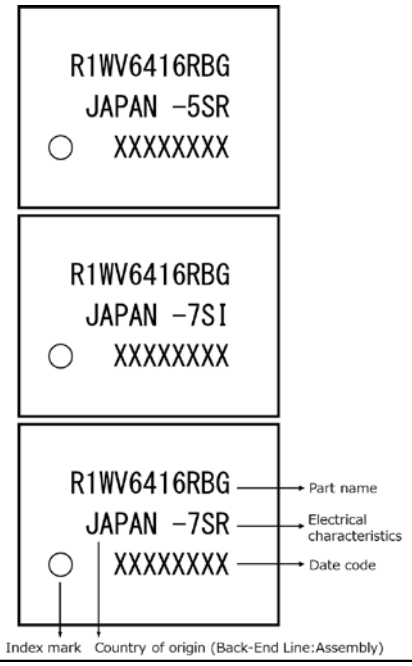
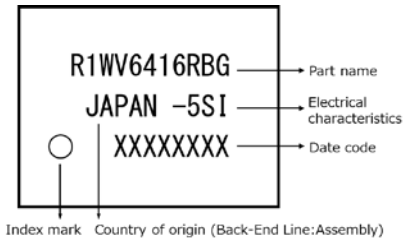
- Note: Accompanied with a change of JEDEC tray, the package seat position in tray pocket is to be changed. Please see page 18.
- Note: Accompanied with a change of embossed tape, the package seat position in taping pocket is not to be changed. No change in width and pitch of embossed tape. No change in reel diameter.

(2) 48pin-TSOP(I) 64Mb(3V) Part name : R1WV6416RSA

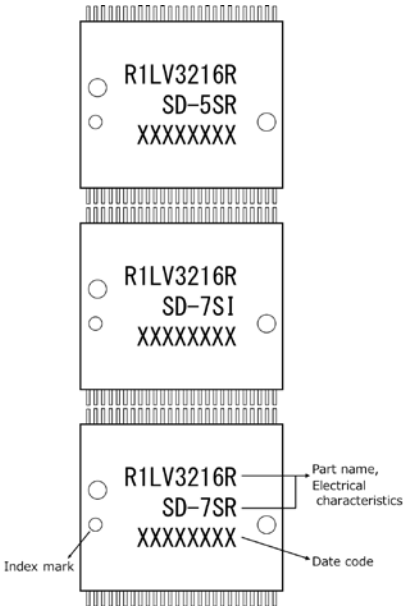
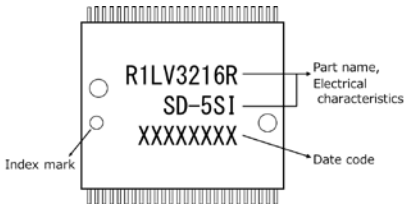
| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1WV6416RSA-5SI/-5SR/-7SI/-7SR#B0 (Tray packing)<br>R1WV6416RSA-5SI/-5SR/-7SI/-7SR#S0 (Tape & Reel packing) | R1WV6416RSA-5SI#B0 (Tray packing)<br>R1WV6416RSA-5SI#S0 (Tape & Reel packing) |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| Country of origin display | | CHINA | ← |
| JEITA Package Code | | P-TSOP(1)48-12x18.4-0.50 | ← |
| Package marking specification | |  |  |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Tray packing | Packing specification | Current specification | New specification |
| | Tray | JEDEC Tray with Renesas Logo<br>(TSOP I package size: 12mm x 18.4mm) | JEDEC Tray without Renesas Logo<br>(TSOP I package size: 12mm x 18.4mm) |
| | Storage number | 96pcs/tray | 96pcs/tray |
| | Laying direction of ICs on a tray | Direction from the top left position to the down side<br>(when the position of chamfer in tray's corner is bottom left.) | No change |
| | Number of trays (Max.) | 8 trays + 1 tray (cover) | 10 trays + 1 tray (cover) |
| | Inner box size (LxWxH) | 330mm x 152mm x 75mm | 351mm x 175mm x 104mm |
| Tape & Reel packing | Packing specification | Current specification | New specification |
| | Embossed tape | Current specification (type name : TE3216-16P) | New specification (type name : TSOP48-3) |
| | Storage number | 1,000pcs/reel | 1,000pcs/reel |
| | Inner box size (LxWxH) | 347mm x 368mm x 54mm | 362mm x 340mm x 60mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

- Note: Accompanied with a change of JEDEC tray, the package seat position in tray pocket is to be changed. Please see page 18.
- Note: Accompanied with a change of embossed tape, the package seat position in taping pocket is not to be changed. No change in width and pitch of embossed tape. No change in reel diameter.

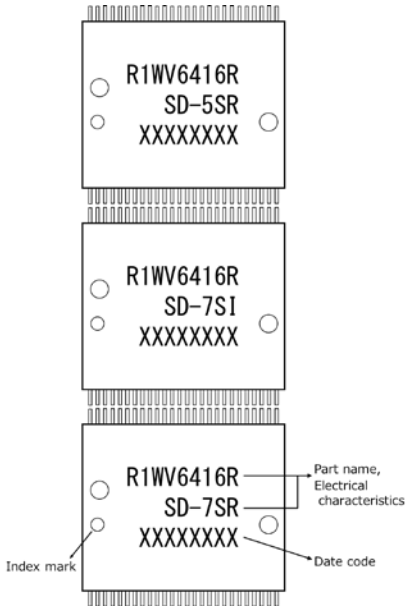
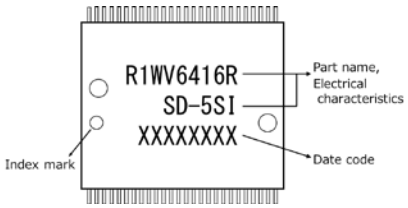
(3) 48ball-FBGA 64Mb(3V) Part name : R1WV6416RBG

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1WV6416RBG-5SR/-7SI/-7SR#B0 (Tray packing) | R1WV6416RBG-5SI#B0 (Tray packing) |
| | | R1WV6416RBG-5SR/-7SI/-7SR#S0 (Tape & Reel packing) | R1WV6416RBG-5SI#S0 (Tape & Reel packing) |
| Assembly line | | J-Devices Kumamoto District (Japan) | ← |
| Country of origin display | | JAPAN | ← |
| JEITA Package Code | | P-TFBGA48-8.5x11-0.75 | ← |
| Package marking specification | |  |  |
| Assembly Material | Substrate material | Glass epoxy | ← |
| | Solder ball | Sn-Ag-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Tray packing | Packing specification | Current specification | New specification |
| | Tray | JEDEC Tray with Renesas Logo<br>(Tray type name : L196-121) | ← |
| | Storage number | 242pcs/tray | ← |
| | Laying direction of ICs on a tray | Direction from the bottm right position to the up side<br>(when the position of chamfer in tray's corner is bottom left.) | Direction from the top left position to the down side<br>(when the position of chamfer in tray's corner is bottom left.) |
| | Number of trays (Max.) | 8 trays + 1 tray (cover) | 10 trays + 1 tray (cover) |
| | Inner box size (LxWxH) | 330mm x 152mm x 75mm | 351mm x 175mm x 104mm |
| Tape & Reel packing | Packing specification | Current specification | New specification |
| | Embossed tape | Current specification | No change |
| | Storage number | 1,000pcs/reel | ← |
| | Inner box size (LxWxH) | 288mm x 273mm x 48mm | 289mm x 264mm x 60mm |
| Moisture-proof performance | | MSL 3 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

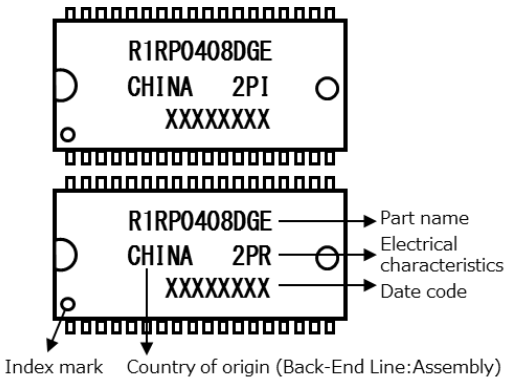
(4) 52pin-µTSOP 32Mb(3V) Part name : R1LV3216RSD

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1LV3216RSD-5SR/-7SI/-7SR#B0 (Tray packing) | R1LV3216RSD-5SI#B0 (Tray packing) |
| | | R1LV3216RSD-5SR/-7SI/-7SR#S0 (Tape & Reel packing) | R1LV3216RSD-5SI#S0 (Tape & Reel packing) |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| JEITA Package Code | | P-TSOP(2)52-8.89x10.79-0.40 | ← |
| Package marking specification | |  |  |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Tray packing | Packing specification | Current specification | New specification |
| | Tray | JEDEC Tray with Renesas Logo<br>(Tray type name : L196-24) | ← |
| | Storage number | 230pcs/tray | ← |
| | Laying direction of ICs on a tray | Direction from the bottm right position to the up side<br>(when the position of chamfer in tray's corner is bottom left.) | Direction from the top left position to the down side<br>(when the position of chamfer in tray's corner is bottom left.) |
| | Number of trays (Max.) | 8 trays + 1 tray (cover) | 10 trays + 1 tray (cover) |
| | Inner box size (LxWxH) | 330mm x 152mm x 75mm | 351mm x 175mm x 104mm |
| Tape & Reel packing | Packing specification | Current specification | New specification |
| | Embossed tape | Current specification | No change |
| | Storage number | 1,000pcs/reel | ← |
| | Inner box size (LxWxH) | 288mm x 273mm x 48mm | 289mm x 264mm x 60mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

(5) 52pin-µTSOP 64Mb(3V) Part name : R1WV6416RSD

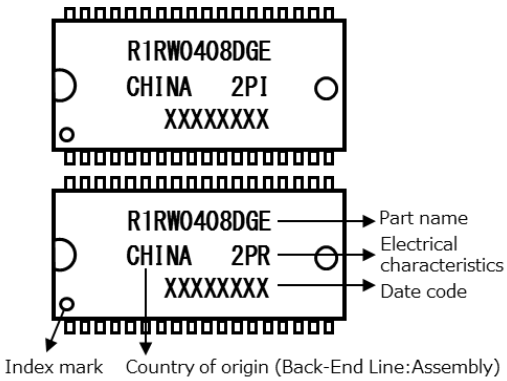
| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1WV6416RSD-5SR/-7SI/-7SR#B0 (Tray packing) | R1WV6416RSD-5SI#B0 (Tray packing) |
| | | R1WV6416RSD-5SR/-7SI/-7SR#S0 (Tape & Reel packing) | R1WV6416RSD-5SI#S0 (Tape & Reel packing) |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| JEITA Package Code | | P-TSOP(2)52-8.89x10.79-0.40 | ← |
| Package marking specification | |  |  |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Tray packing | Packing specification | Current specification | New specification |
| | Tray | JEDEC Tray with Renesas Logo<br>(Tray type name : L196-24) | ← |
| | Storage number | 230pcs/tray | ← |
| | Laying direction of ICs on a tray | Direction from the bottm right position to the up side<br>(when the position of chamfer in tray's corner is bottom left.) | Direction from the top left position to the down side<br>(when the position of chamfer in tray's corner is bottom left.) |
| | Number of trays (Max.) | 8 trays + 1 tray (cover) | 10 trays + 1 tray (cover) |
| | Inner box size (LxWxH) | 330mm x 152mm x 75mm | 351mm x 175mm x 104mm |
| Tape & Reel packing | Packing specification | Current specification | New specification |
| | Embossed tape | Current specification | No change |
| | Storage number | 1,000pcs/reel | ← |
| | Inner box size (LxWxH) | 288mm x 273mm x 48mm | 289mm x 264mm x 60mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

(6) 36pin-SOJ 4Mb Fast(5V) x8 Part name : R1RP0408DGE

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1RP0408DGE-0PI/-0PR/-2LR/-2PI/-2PR#B0 (Magazine packing) | ← |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| Country of origin display | | CHINA | ← |
| JEITA Package Code | | P-SOJ36-10.16x23.39-1.27 | ← |
| Package marking specification (The Electrical characteristics is an example.) | |  | No change |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Magazine packing | Packing specification | Current specification | New specification |
| | Magazine | Magagine code : JP400PC | ← |
| | Storage number | 22pcs/magazine | ← |
| | Number of magazines (Max.) | 60 magazines | ← |
| | Inner box size (LxWxH) | 600mm x 172mm x 77mm | 595mm x 170mm x 72mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

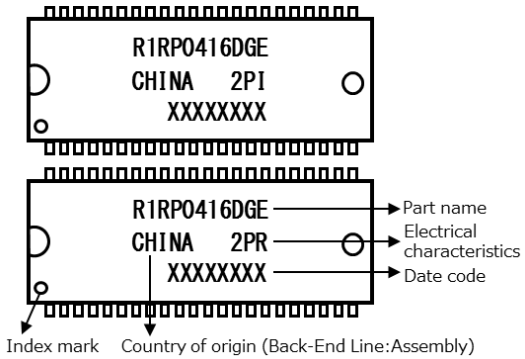
- Regarding R1RP0408DGE, laser marking on the package's surface is processed at final test site.

(7) 36pin-SOJ 4Mb Fast(3V) x8 Part name : R1RW0408DGE

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1RW0408DGE-0PI/-0PR/-2LR/-2PI/2PR#B0 (Magazine packing) | ← |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| Country of origin display | | CHINA | ← |
| JEITA Package Code | | P-SOJ36-10.16x23.39-1.27 | ← |
| Package marking specification (The Electrical characteristics is an example.) | |  | No change |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Magazine packing | Packing specification | Current specification | New specification |
| | Magazine | Magagine code : JP400PC | ← |
| | Storage number | 22pcs/magazine | ← |
| | Number of magazines (Max.) | 60 magazines | ← |
| | Inner box size (LxWxH) | 600mm x 172mm x 77mm | 595mm x 170mm x 72mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

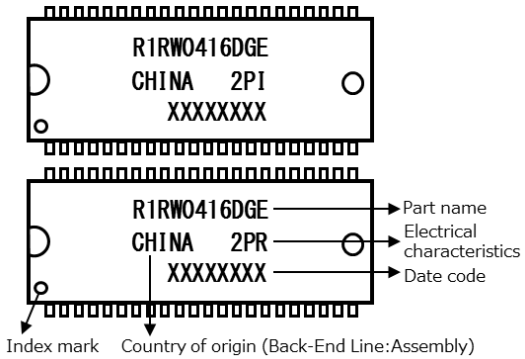
- Regarding R1RW0408DGE, laser marking on the package's surface is processed at final test site.

(8) 44pin-SOJ 4Mb Fast(5V) x16 Part name : R1RP0416DGE

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1RP0416DGE<br>-0PR/-2LR/-2PI/-2PR/-2SR/-2UR/-2VR#B0 (Magazine packing) | ← |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| Country of origin display | | CHINA | ← |
| JEITA Package Code | | P-SOJ44-10.16x28.47-1.27 | ← |
| Package marking specification (The Electrical characteristics is an example.) | |  | No change |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Magazine packing | Packing specification | Current specification | New specification |
| | Magazine | Magagine code : JP400PC | ← |
| | Storage number | 18pcs/magazine | ← |
| | Number of magazines (Max.) | 60 magazines | ← |
| | Inner box size (LxWxH) | 600mm x 172mm x 77mm | 595mm x 170mm x 72mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

- Regarding R1RP0416DGE, laser marking on the package's surface is processed at final test site.

(9) 44pin-SOJ 4Mb Fast(3V) x16 Part name : R1RW0416DGE

| Item | | Pre Change | Post Change |
|---|---|---|---|
| Orderable part name | | R1RW0416DGE<br>-0PR/-2LR/-2PI/-2PR/-2SR/-2UR#B0 (Magazine packing) | ← |
| Assembly line | | Renesas Semiconductor Beijing (China) | ← |
| Country of origin display | | CHINA | ← |
| JEITA Package Code | | P-SOJ44-10.16x28.47-1.27 | ← |
| Package marking specification (The Electrical characteristics is an example.) | |  | No change |
| Assembly Material | Lead frame material | 42Alloy | ← |
| | Lead plating | Sn-Cu | ← |
| | Die bonding | Epoxy film | ← |
| | Wire bonding | Au | ← |
| | Mold | Epoxy resin (Halogen-included) | ← |
| Final test line | | Renesas Semiconductor Beijing (China) | Powertech Technology Inc. (Taiwan) |
| Magazine packing | Packing specification | Current specification | New specification |
| | Magazine | Magagine code : JP400PC | ← |
| | Storage number | 18pcs/magazine | ← |
| | Number of magazines (Max.) | 60 magazines | ← |
| | Inner box size (LxWxH) | 600mm x 172mm x 77mm | 595mm x 170mm x 72mm |
| Moisture-proof performance | | MSL 2 | ← |
| Shipping label | | Current specification | No change in format (Changes in Renesas internal code) |

- Regarding R1RW0416DGE, laser marking on the package's surface is processed at final test site.

## 3. Product integration by EOL of “-5SR, -7SI, -7SR” products ( for 32Mb / 64Mb Low Power SRAM )

- Regarding the EOL of “-5SR, -7SI, -7SR” products, these "Access and Temperature grades" are unified to "-5SI" (see below).

| Package Type | Memory Cap., Supply Voltage | bit | Pre Change | | | Post Change | | |
|---|---|---|---|---|---|---|---|---|
| | | | Orderable Part Name | Access time | Operation Temp. | Orderable Part Name | Access time | Operation Temp. |
| 48pin-TSOP(I) | 32Mb 3V | x16 | R1LV3216RSA-5SR#B0<br>R1LV3216RSA-5SR#S0 | 55ns | 0℃ ～70℃ | R1LV3216RSA-5SI#B1<br>R1LV3216RSA-5SI#S1 | 55ns | -40℃ ～85℃ |
| | | | R1LV3216RSA-7SI#B0<br>R1LV3216RSA-7SI#S0 | 70ns | -40℃ ～85℃ | | | |
| | | | R1LV3216RSA-7SR#B0<br>R1LV3216RSA-7SR#S0 | | 0℃ ～70℃ | | | |
| | 64Mb 3V | x16 | R1WV6416RSA-5SI#B0<br>R1WV6416RSA-5SI#S0 | 55ns | -40℃ ～85℃ | R1WV6416RSA-5SI#B0<br>R1WV6416RSA-5SI#S0 | 55ns | -40℃ ～85℃ |
| | | | R1WV6416RSA-5SR#B0<br>R1WV6416RSA-5SR#S0 | | -0℃ ～70℃ | | | |
| | | | R1WV6416RSA-7SI#B0<br>R1WV6416RSA-7SI#S0 | 70ns | -40℃ ～85℃ | | | |
| | | | R1WV6416RSA-7SR#B0<br>R1WV6416RSA-7SR#S0 | | 0℃ ～70℃ | | | |
| 48ball-FBGA | 64Mb 3V | x16 | R1WV6416RBG-5SR#B0<br>R1WV6416RBG-5SR#S0 | 55ns | 0℃ ～70℃ | R1WV6416RBG-5SI#B0<br>R1WV6416RBG-5SI#S0 | 55ns | -40℃ ～85℃ |
| | | | R1WV6416RBG-7SI#B0<br>R1WV6416RBG-7SI#S0 | 70ns | -40℃ ～85℃ | | | |
| | | | R1WV6416RBG-7SR#B0<br>R1WV6416RBG-7SR#S0 | | 0℃ ～70℃ | | | |
| 52pin-μTSOP | 32Mb 3V | x16 | R1LV3216RSD-5SR#B0<br>R1LV3216RSD-5SR#S0 | 55ns | 0℃ ～70℃ | R1LV3216RSD-5SI#B0<br>R1LV3216RSD-5SI#S0 | 55ns | -40℃ ～85℃ |
| | | | R1LV3216RSD-7SI#B0<br>R1LV3216RSD-7SI#S0 | 70ns | -40℃ ～85℃ | | | |
| | | | R1LV3216RSD-7SR#B0<br>R1LV3216RSD-7SR#S0 | | 0℃ ～70℃ | | | |
| | 64Mb 3V | x16 | R1WV6416RSD-5SR#B0<br>R1WV6416RSD-5SR#S0 | 55ns | 0℃ ～70℃ | R1WV6416RSD-5SI#B0<br>R1WV6416RSD-5SI#S0 | 55ns | -40℃ ～85℃ |
| | | | R1WV6416RSD-7SI#B0<br>R1WV6416RSD-7SI#S0 | 70ns | -40℃ ～85℃ | | | |
| | | | R1WV6416RSD-7SR#B0<br>R1WV6416RSD-7SR#S0 | | 0℃ ～70℃ | | | |

- #B0, #B1: Tray packing, #S0, #S1: Tape & Reel packing.

# 4. Electrical characteristics (DC/AC) (for 32Mb / 64Mb Low Power SRAM)

- Regarding the EOL of “-5SR, -7SI, -7SR” products, electrical characteristics (DC/AC) of unified “-5SI” product is completely upper-compatible with “- “-5SR, -7SI, -7SR” products (see below).

## (1)–a. Electrical characteristics (DC) : 32Mb(3V) R1LV3216RSA, R1LV3216RSD

Products

| Item | **Pre Change** | **Post Change** |
|---|---|---|
| Orderable part name | R1LV3216RSA-5SR, -7SI, -7SR#B0 | R1LV3216RSA-5SI#B1 |
| | R1LV3216RSA-5SR, -7SI, -7SR#S0 | R1LV3216RSA-5SI#S1 |
| | R1LV3216RSD-5SR, -7SI, -7SR#B0 | R1LV3216RSD-5SI#B0 |
| | R1LV3216RSD-5SR, -7SI, -7SR#S0 | R1LV3216RSD-5SI#S0 |

DC conditions

| Item | Symbol | **Pre Change** | | Symbol | **Post Change** |
|---|---|---|---|---|---|
| Supply voltage | Vcc | 2.7V～3.6V | | Vcc | ← |
| Operating temperature range | Ta | 5SR, 7SR | 0℃～70℃ | Ta | -40℃～85℃ |
| | | 7SI | -40℃～85℃ | | |
| Input high voltage | VIH | 2.4V(min.) / Vcc+0.2V(max.) | | VIH | ← |
| Input low voltage | VIL | -0.2V(min.) / 0.4V(max.) | | VIL | ← |

DC characteristics

| Item | Symbol | **Pre Change** | | Symbol | **Post Change** | |
|---|---|---|---|---|---|---|
| Operating Current | Icc1(TTL, Min.Cycle) | 55mA(max.) / 40mA(typ.) | | Icc1(TTL, Min.Cycle) | ← | |
| | Icc2(MOS, Cycle=1us) | 8mA(max.) / 3mA(typ.) | | Icc2(MOS, Cycle=1us) | ← | |
| Standby current | ISB(TTL) | 0.3mA(max.) / 0.1mA(typ.) | | ISB(TTL) | ← | |
| | ISB1(MOS) | ～25℃ | 12uA(max.) / 4uA(typ.) | ISB1(MOS) | ～25℃ | ← |
| | | ～40℃ | 24uA(max.) / 7uA(typ.) | | ～40℃ | ← |
| | | ～70℃ | 50uA(max.) | | ～70℃ | ← |
| | | ～85℃ (for 7SI) | 80uA(max.) | | ～85℃ | ← |
| Output high voltage | VOH | IOH=-0.5mA | 2.4V(min.) | VOH | IOH=-0.5mA | ← |
| Output low voltage | VOL | IOL=2mA | 0.4V(max.) | VOL | IOL=2mA | ← |

Capacitance

| Item | Symbol | **Pre Change** | Symbol | **Post Change** |
|---|---|---|---|---|
| Input capacitance | C in | 10pF(max.) | C in | ← |
| Input/Output capacitance | C I/O | 10pF(max.) | C I/O | ← |

Data retention characteristics

| Item | Symbol | **Pre Change** | | Symbol | **Post Change** | |
|---|---|---|---|---|---|---|
| Vcc for data retention | VDR | 2.0V(min.) | | VDR | ← | |
| Data retention current | IccDR | ～25℃ | 12uA(max.) / 4uA(typ.) | IccDR | ～25℃ | ← |
| | | ～40℃ | 24uA(max.) / 7uA(typ.) | | ～40℃ | ← |
| | | ～70℃ | 50uA(max.) | | ～70℃ | ← |
| | | ～85℃ (for 7SI) | 80uA(max.) | | ～85℃ | ← |
| Chip deselect time to data retention | tCDR | 0ns(min.) | | tCDR | ← | |
| Operation recovery time | tR | 5ms(min.) | | tR | ← | |

## (1)–b. Electrical characteristics (AC) : 32Mb(3V) R1LV3216RSA, R1LV3216RSD

Products

| Item | Pre Change | Post Change |
|---|---|---|
| Orderable part name | R1LV3216RSA-5SR, -7SI, -7SR#B0 | R1LV3216RSA-5SI#B1 |
| | R1LV3216RSA-5SR, -7SI, -7SR#S0 | R1LV3216RSA-5SI#S1 |
| | R1LV3216RSD-5SR, -7SI, -7SR#B0 | R1LV3216RSD-5SI#B0 |
| | R1LV3216RSD-5SR, -7SI, -7SR#S0 | R1LV3216RSD-5SI#S0 |

AC characteristics
Read Cycle

| Item | Symbol | Pre Change | | Symbol | Post Change |
|---|---|---|---|---|---|
| Read cycle time | tRC | 5SR | 55ns(min.) | tRC | 55ns(min.) |
| | | 7SI, 7SR | 70ns(min.) | | |
| Address access time | tAA | 5SR | 55ns(max.) | tAA | 55ns(max.) |
| | | 7SI, 7SR | 70ns(max.) | | |
| Chip select access time | tACS1 / tACS2 | 5SR | 55ns(max.) | tACS1 / tACS2 | 55ns(max.) |
| | | 7SI, 7SR | 70ns(max.) | | |
| Output enable to output valid | tOE | 5SR | 25ns(max.) | tOE | 25ns(max.) |
| | | 7SI, 7SR | 35ns(max.) | | |
| Output hold from address change | tOH | 5SR | 10ns(min.) | tOH | ← |
| | | 7SI, 7SR | 10ns(min.) | | |
| LB#,UB# access time | tBA | 5SR | 55ns(max.) | tBA | 55ns(max.) |
| | | 7SI, 7SR | 70ns(max.) | | |
| Chip select to output in low-Z | tCLZ1 / tCLZ2 | 5SR | 10ns(min.) | tCLZ1 / tCLZ2 | ← |
| | | 7SI, 7SR | 10ns(min.) | | |
| LB#,UB# enable to low-Z | tBLZ | 5SR | 5ns(min.) | tBLZ | ← |
| | | 7SI, 7SR | 5ns(min.) | | |
| Output enable to output in low-Z | tOLZ | 5SR | 5ns(min.) | tOLZ | ← |
| | | 7SI, 7SR | 5ns(min.) | | |
| Chip deselect to output in high-Z | tCHZ1 / tCHZ2 | 5SR | 0ns(min.) / 20ns(max.) | tCHZ1 / tCHZ2 | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |
| LB#,UB# disable to high-Z | tBHZ | 5SR | 0ns(min.) / 20ns(max.) | tBHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |
| Output disable to output in high-Z | tOHZ | 5SR | 0ns(min.) / 20ns(max.) | tOHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |

Write Cycle

| Item | Symbol | Pre Change | | Symbol | Post Change |
|---|---|---|---|---|---|
| Write cycle time | tWC | 5SR | 55ns(min.) | tWC | 55ns(min.) |
| | | 7SI, 7SR | 70ns(min.) | | |
| Address valid to end of write | tAW | 5SR | 50ns(min.) | tAW | 50ns(min.) |
| | | 7SI, 7SR | 65ns(min.) | | |
| Chip select to end of write | tCW | 5SR | 50ns(min.) | tCW | 50ns(min.) |
| | | 7SI, 7SR | 65ns(min.) | | |
| Write pulse width | tWP | 5SR | 40ns(min.) | tWP | 40ns(min.) |
| | | 7SI, 7SR | 55ns(min.) | | |
| LB#,UB# valid to end of write | tBW | 5SR | 50ns(min.) | tBW | 50ns(min.) |
| | | 7SI, 7SR | 65ns(min.) | | |
| Address setup time | tAS | 5SR | 0ns(min.) | tAS | ← |
| | | 7SI, 7SR | 0ns(min.) | | |
| Write recovery time | tWR | 5SR | 0ns(min.) | tWR | ← |
| | | 7SI, 7SR | 0ns(min.) | | |
| Data to write time overlap | tDW | 5SR | 25ns(min.) | tDW | 25ns(min.) |
| | | 7SI, 7SR | 35ns(min.) | | |
| Data hold from write time | tDH | 5SR | 0ns(min.) | tDH | ← |
| | | 7SI, 7SR | 0ns(min.) | | |
| Output enable from end of write | tOW | 5SR | 5ns(min.) | tOW | ← |
| | | 7SI, 7SR | 5ns(min.) | | |
| Output disable to output in high-Z | tOHZ | 5SR | 0ns(min.) / 20ns(max.) | tOHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |
| Write to output in high-Z | tWHZ | 5SR | 0ns(min.) / 20ns(max.) | tWHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |

## (2)–a. Electrical characteristics (DC) : 64Mb(3V) R1WV6416RSA, R1WV6416RBG, R1WV6416RSD

Products

| Item | Pre Change | Post Change |
|---|---|---|
| Orderable part name | R1WV6416RSA-5SI, 5SR, -7SI, -7SR#B0 | R1WV6416RSA-5SI#B0 |
| | R1WV6416RSA-5SI, 5SR, -7SI, -7SR#S0 | R1WV6416RSA-5SI#S0 |
| | R1WV6416RBG-5SR, -7SI, -7SR#B0 | R1WV6416RBG-5SI#B0 |
| | R1WV6416RBG-5SR, -7SI, -7SR#S0 | R1WV6416RBG-5SI#S0 |
| | R1WV6416RSD-5SR, -7SI, -7SR#B0 | R1WV6416RSD-5SI#B0 |
| | R1WV6416RSD-5SR, -7SI, -7SR#S0 | R1WV6416RSD-5SI#S0 |

DC conditions

| Item | Symbol | Pre Change | | Symbol | Post Change |
|---|---|---|---|---|---|
| Supply voltage | Vcc | 2.7V～3.6V | | Vcc | ← |
| Operating temperature range | Ta | 5SR, 7SR | 0℃～70℃ | Ta | -40℃～85℃ |
| | | 5SI, 7SI | -40℃～85℃ | | |
| Input high voltage | VIH | 2.4V(min.) / Vcc+0.2V(max.) | | VIH | ← |
| Input low voltage | VIL | -0.2V(min.) / 0.4V(max.) | | VIL | ← |

DC characteristics

| Item | Symbol | Pre Change | | Symbol | Post Change | |
|---|---|---|---|---|---|---|
| Operating Current | Icc1(TTL, Min.Cycle) | 60mA(max.) / 45mA(typ.) | | Icc1(TTL, Min.Cycle) | ← | |
| | Icc2(MOS, Cycle=1us) | 10mA(max.) / 5mA(typ.) | | Icc2(MOS, Cycle=1us) | ← | |
| Standby current | ISB(TTL) | 0.3mA(max.) / 0.1mA(typ.) | | ISB(TTL) | ← | |
| | ISB1(MOS) | ～25℃ | 24uA(max.) / 8uA(typ.) | ISB1(MOS) | ～25℃ | ← |
| | | ～40℃ | 48uA(max.) / 14uA(typ.) | | ～40℃ | ← |
| | | ～70℃ | 100uA(max.) | | ～70℃ | ← |
| | | ～85℃ (for 5SI, 7SI) | 160uA(max.) | | ～85℃ | ← |
| Output high voltage | VOH | IOH=-0.5mA | 2.4V(min.) | VOH | IOH=-0.5mA | ← |
| Output low voltage | VOL | IOL=2mA | 0.4V(max.) | VOL | IOL=2mA | ← |

Capacitance

| Item | Symbol | Pre Change | Symbol | Post Change |
|---|---|---|---|---|
| Input capacitance | C in | 20pF(max.) | C in | ← |
| Input/Output capacitance | C I/O | 20pF(max.) | C I/O | ← |

Data retention characteristics

| Item | Symbol | Pre Change | | Symbol | Post Change | |
|---|---|---|---|---|---|---|
| Vcc for data retention | VDR | 2.0V(min.) | | VDR | ← | |
| Data retention current | IccDR | ～25℃ | 24uA(max.) / 8uA(typ.) | IccDR | ～25℃ | ← |
| | | ～40℃ | 48uA(max.) / 14uA(typ.) | | ～40℃ | ← |
| | | ～70℃ | 100uA(max.) | | ～70℃ | ← |
| | | ～85℃ (for 5SI, 7SI) | 160uA(max.) | | ～85℃ | ← |
| Chip deselect time to data retention | tCDR | 0ns(min.) | | tCDR | ← | |
| Operation recovery time | tR | 5ms(min.) | | tR | ← | |

## (2)–b. Electrical characteristics (AC) : 64Mb(3V) R1WV6416RSA, R1WV6416RBG, R1WV6416RSD

Products

| Item | Pre Change | Post Change |
|---|---|---|
| Orderable part name | R1WV6416RSA-5SI, 5SR, -7SI, -7SR#B0 | R1WV6416RSA-5SI#B0 |
| | R1WV6416RSA-5SI, 5SR, -7SI, -7SR#S0 | R1WV6416RSA-5SI#S0 |
| | R1WV6416RBG-5SR, -7SI, -7SR#B0 | R1WV6416RBG-5SI#B0 |
| | R1WV6416RBG-5SR, -7SI, -7SR#S0 | R1WV6416RBG-5SI#S0 |
| | R1WV6416RSD-5SR, -7SI, -7SR#B0 | R1WV6416RSD-5SI#B0 |
| | R1WV6416RSD-5SR, -7SI, -7SR#S0 | R1WV6416RSD-5SI#S0 |

AC characteristics

Read Cycle

| Item | Symbol | Pre Change | | Symbol | Post Change |
|---|---|---|---|---|---|
| Read cycle time | tRC | 5SI, 5SR | 55ns(min.) | tRC | 55ns(min.) |
| | | 7SI, 7SR | 70ns(min.) | | |
| Address access time | tAA | 5SI, 5SR | 55ns(max.) | tAA | 55ns(max.) |
| | | 7SI, 7SR | 70ns(max.) | | |
| Chip select access time | tACS1 / tACS2 | 5SI, 5SR | 55ns(max.) | tACS1 / tACS2 | 55ns(max.) |
| | | 7SI, 7SR | 70ns(max.) | | |
| Output enable to output valid | tOE | 5SI, 5SR | 25ns(max.) | tOE | 25ns(max.) |
| | | 7SI, 7SR | 35ns(max.) | | |
| Output hold from address change | tOH | 5SI, 5SR | 10ns(min.) | tOH | ← |
| | | 7SI, 7SR | 10ns(min.) | | |
| LB#,UB# access time | tBA | 5SI, 5SR | 55ns(max.) | tBA | 55ns(max.) |
| | | 7SI, 7SR | 70ns(max.) | | |
| Chip select to output in low-Z | tCLZ1 / tCLZ2 | 5SI, 5SR | 10ns(min.) | tCLZ1 / tCLZ2 | ← |
| | | 7SI, 7SR | 10ns(min.) | | |
| LB#,UB# enable to low-Z | tBLZ | 5SI, 5SR | 5ns(min.) | tBLZ | ← |
| | | 7SI, 7SR | 5ns(min.) | | |
| Output enable to output in low-Z | tOLZ | 5SI, 5SR | 5ns(min.) | tOLZ | ← |
| | | 7SI, 7SR | 5ns(min.) | | |
| Chip deselect to output in high-Z | tCHZ1 / tCHZ2 | 5SI, 5SR | 0ns(min.) / 20ns(max.) | tCHZ1 / tCHZ2 | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |
| LB#,UB# disable to high-Z | tBHZ | 5SI, 5SR | 0ns(min.) / 20ns(max.) | tBHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |
| Output disable to output in high-Z | tOHZ | 5SI, 5SR | 0ns(min.) / 20ns(max.) | tOHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |

Write Cycle

| Item | Symbol | Pre Change | | Symbol | Post Change |
|---|---|---|---|---|---|
| Write cycle time | tWC | 5SI, 5SR | 55ns(min.) | tWC | 55ns(min.) |
| | | 7SI, 7SR | 70ns(min.) | | |
| Address valid to end of write | tAW | 5SI, 5SR | 50ns(min.) | tAW | 50ns(min.) |
| | | 7SI, 7SR | 65ns(min.) | | |
| Chip select to end of write | tCW | 5SI, 5SR | 50ns(min.) | tCW | 50ns(min.) |
| | | 7SI, 7SR | 65ns(min.) | | |
| Write pulse width | tWP | 5SI, 5SR | 40ns(min.) | tWP | 40ns(min.) |
| | | 7SI, 7SR | 55ns(min.) | | |
| LB#,UB# valid to end of write | tBW | 5SI, 5SR | 50ns(min.) | tBW | 50ns(min.) |
| | | 7SI, 7SR | 65ns(min.) | | |
| Address setup time | tAS | 5SI, 5SR | 0ns(min.) | tAS | ← |
| | | 7SI, 7SR | 0ns(min.) | | |
| Write recovery time | tWR | 5SI, 5SR | 0ns(min.) | tWR | ← |
| | | 7SI, 7SR | 0ns(min.) | | |
| Data to write time overlap | tDW | 5SI, 5SR | 25ns(min.) | tDW | 25ns(min.) |
| | | 7SI, 7SR | 35ns(min.) | | |
| Data hold from write time | tDH | 5SI, 5SR | 0ns(min.) | tDH | ← |
| | | 7SI, 7SR | 0ns(min.) | | |
| Output enable from end of write | tOW | 5SI, 5SR | 5ns(min.) | tOW | ← |
| | | 7SI, 7SR | 5ns(min.) | | |
| Output disable to output in high-Z | tOHZ | 5SI, 5SR | 0ns(min.) / 20ns(max.) | tOHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |
| Write to output in high-Z | tWHZ | 5SI, 5SR | 0ns(min.) / 20ns(max.) | tWHZ | 0ns(min.) / 20ns(max.) |
| | | 7SI, 7SR | 0ns(min.) / 25ns(max.) | | |

## 5. Packing specification (tray shipping)

(1) Change the specification of the JEDEC tray（48pin-TSOP(I) products only）

- Regarding 48pin-TSOP(I) products (R1LV3216RSA and R1WV6416RSA), the package seat position in tray pocket is to be changed (see below).

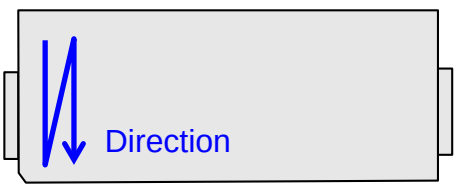
  No change in outline dimensions and pocket pitch for JEDEC tray.
- Regarding other products (48ball-FBGA, 52pin-μTSOP), no change in the JEDEC tray.

| Package type | Pre Change | | Post Change | |
|---|---|---|---|---|
| | Tray type name | PKG seat position (mm) | Tray type name | PKG seat position (mm) |
| 48pin-TSOP(I) | L196-126 | 2.0 | EA51220 | 1.5 |


Cross section of tray pocket

(2) Laying direction of ICs on a tray

- Regarding 48ball-FBGA products (R1WV6416RBG) and 52pin-μTSOP (R1LV3216RSD, R1WV6416RSD), laying direction of ICs on a tray is to be changed (see below).
- No change in other products, because the direction is already same as the "Post Change“ as shown below.

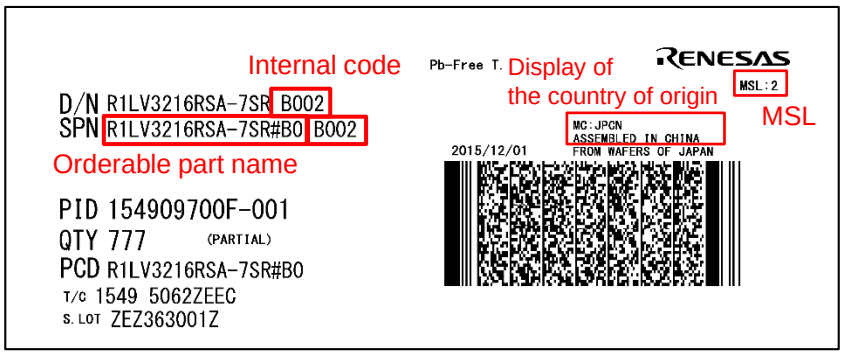
| | Pre Change | Post Change |
|---|---|---|
| Laying direction of ICs on a tray |   |   |
| Orderable part name | R1WV6416RBG-5SR/-7SI/-7SR#B0<br>R1LV3216RSD-5SR/-7SI/-7SR#B0<br>R1WV6416RSD-5SR/-7SI/-7SR#B0 | R1WV6416RBG-5SI#B0<br>R1LV3216RSD-5SI#B0<br>R1WV6416RSD-5SI#B0 |

## 6. Shipping label

- Label format itself is not changed.
- Written specifications: “Internal code“ is changed. See below for example.
  ( Note: Regarding R1LV3216RSA, “the country of origin" and MSL are changed. )

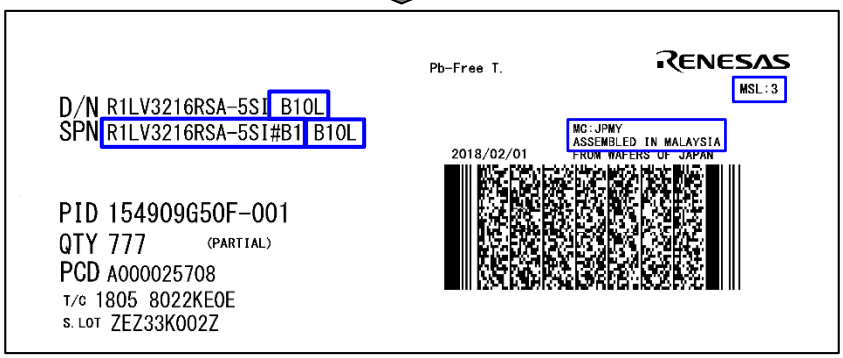
(1) R1LV3216RSA
(-5SR, -7SI, -7SR)

Pre Change



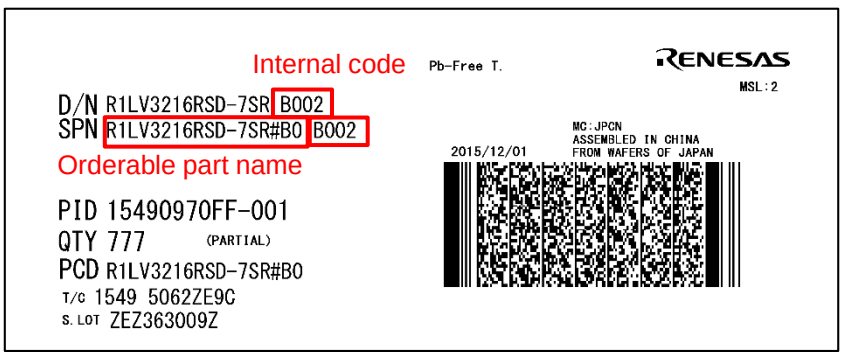

Note: Orderable part name is changed to “-5SI”.

Post Change




(2) Example of a EOL product
(-5SR, -7SI, -7SR)
except R1LV3216RSA

Pre Change

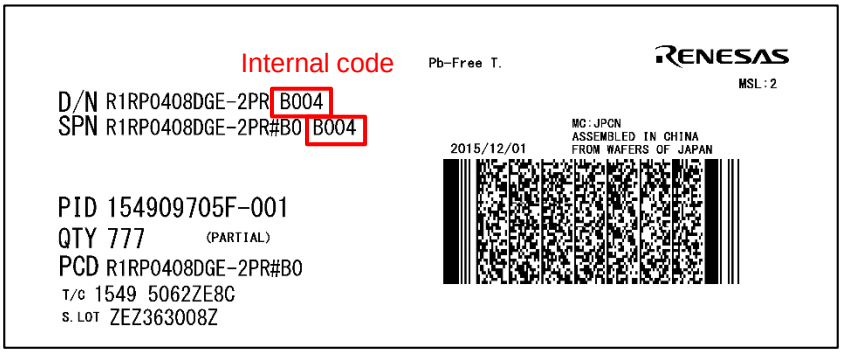



Note: Orderable part name is changed to “-5SI”.

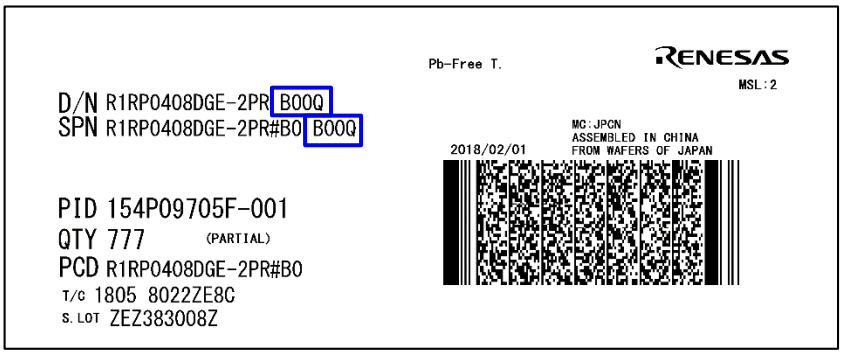
Post Change

(3) Example of a product whose orderable part name is not changed.

Pre Change




Post Change




## 7. Site information

- Final-test site information of the post-change products is as follows.

  <Final-Test Site>

  Company Name : Powertech Technology Inc.

  Country Name : Taiwan

  Company Address : No.10, Datong Rd., Hsinchu Industrial Park, Hukou, Hsinchu 30352, Taiwan
  (for 48pin-TSOP(I), 48ball-FBGA, 52pin-µTSOP)

  No.879, Litoushan Sec., Wunshan Rd., Hsinpu, Hsinchu 30550, Taiwan
  (for 36pin-SOJ, 44pin-SOJ)

- Only regarding R1LV3216RSA (32Mb 48pin-TSOP(I)), the site of assembly process is changed.

  <Assembly Site>

  Orderable part name of post-change product : R1LV3216RSA-5SI#B1 / #S1

  Company Name : Amkor Technology Malaysia Sdn,Bhd.

  Country Name : Malaysia

  Company Address : 15km, Jalan Klang-Banting, 42507 Telok Panglima Garang, Kuala Langat, Selangor Darul Ehsan, Malaysia

- Regarding other products except R1LV3216RSA (32Mb 48pin-TSOP(I)), the site of assembly process is not changed. Please see pp.5-12.