Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA - 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **TB1812-01** DATE: **January 8, 2019**

Product Affected: F2270NLGK
F2270NLGK8

Date Effective: **April 8, 2019**

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ☐ Product Mark
- ☐ Back Mark
- ☐ Date Code
- ■ Other — Shipment after PCN Effective

Contact: IDT PCN DESK

E-mail: pcndesk@idt.com

Attachment: ■ Yes ☐ No

Samples: Contact your local sales representative for sample and datasheet requests.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ■ Other - ATE limits

This notice is to advise our customers that Data Sheet limits and ATE limits are being changed as the process variation for Control Pin Leakage Current that was used to calculate the original ATE limits does not accurately represent the variation observed in production test measurements.

Refer to Attachment I for details of the changes.

RELIABILITY/QUALIFICATION SUMMARY:

There is no expected change in quality or reliability.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT I - PCN # : TB1812-01

PCN Type: Data Sheet & ATE Limits

Data Sheet Change: Yes

Details Of Change:

This notice is to advise our customers that Data Sheet limits and ATE limits are being changed as the process variation for Control Pin Leakage Current that was used to calculate the original ATE limits does not accurately represent the variation observed in production test measurements.

Table 1: Datasheet Limits Changes

From:

(i) V_{MODE} Current and V_{CTRL} Current

Table 4. Electrical Characteristics (General)

Refer to the application circuit in Figure 60 for the required circuit and use L1 = L2 = 0Ω. The specifications in this table apply at V_{DD} = +5.0V, T_{EP} = +25°C, f_{RF} = 500MHz, $Z_S = Z_L$ = 75Ω, signal applied to RF1, minimum attenuation, P_{IN} = 0dBm for small signal parameters, P_{IN} = +20dBm per tone for two tone tests, V_{MODE} is LOW or HIGH, and Evaluation Board (EVK(t) trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
V_{MODE} Logic Input HIGH	V_{IH}	3.9V ≤ V_{DD} ≤ 5.5V	***1.07*** [a]		3.6	V
		V_{DD} < 3.9V	***1.07***		***V_{DD} – 0.3***	
V_{MODE} Logic Input LOW	V_{IL}		0		***0.63***	V
V_{DD} Current	I_{DD}			1.4	***2.5***	mA
V_{MODE} Current	I_{MODE}		***-40***		***40***	µA
V_{CTRL} Current	I_{CTRL}		***-50***		***50***	µA
Attenuation Slope	ATT_{SLOPE}	V_{MODE} = LOW		10		dB/V
		V_{MODE} = HIGH		-10		
Attenuation Variation over Temperature (reference to +25°C)	ATT_{VAR}	f_{RF} = 50MHz (-40°C to 105°C, over full signal range of V_{CTRL})		±1		dB
Settling Time	t_{SETTLE}	Any 1dB step in the 0dB to 33dB control range, 50% of V_{CTRL} signal to RF settled to within ± 0.1dB		25		µs

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

To:

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
V_{MODE} Logic Input HIGH	V_{IH}	3.9V ≤ V_{DD} ≤ 5.5V	***1.07*** [a]		3.6	V
		V_{DD} < 3.9V	***1.07***		***V_{DD} – 0.3***	
V_{MODE} Logic Input LOW	V_{IL}		0		***0.63***	V
V_{DD} Current	I_{DD}			1.4	***2.5***	mA
V_{MODE} Current	I_{MODE}			25		µA
V_{CTRL} Current	I_{CTRL}			50		µA
Attenuation Slope	ATT_{SLOPE}	V_{MODE} = LOW		10		dB/V
		V_{MODE} = HIGH		-10		
Attenuation Variation over Temperature (reference to +25°C)	ATT_{VAR}	f_{RF} = 50MHz (-40°C to 105°C, over full signal range of V_{CTRL})		±1		dB
Settling Time	t_{SETTLE}	Any 1dB step in the 0dB to 33dB control range, 50% of V_{CTRL} signal to RF settled to within ± 0.1dB		25		µs

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

ATTACHMENT I - PCN # : TB1812-01

Table 2: ATE Limits Changes

(ii) Deleted 3.6v logic current tests

From	To
Test 301 Ictrl @ 3.6v Min 25uA Max 32uA	-
Test 302 Ictrl @ 3.6v Min 8uA Max 30uA	-
Test 303 Ictrl @ 5.5v Min 40uA Max 50uA	Test 303 Ictrl @ 5.5v Min 40uA Max 63uA
Test 401 Ictrl @ 3.6v Min -6uA Max -0.1uA	-
Test 402 Imode @ 3.6v Min -0.9uA Max 0.9uA	-