

## Product Change Notice (PCN)

**Subject:** Datasheet and Wafer Fabrication Site Change for the Listed Intersil EL4340\* Products – NXP Semiconductor Nijmegen, Netherlands

**Publication Date:** 10/5/2017

**Effective Date:** 1/5/2018

**Revision Description:**

Revision 0: Initial Release

**Description of Change:**

This notice is to inform you that Intersil has qualified the NXP Semiconductor facility in Nijmegen, Netherlands for wafer fabrication of the EL4340\* HS6 technology product. The data sheet has been updated to align the specification with the characteristics of the product. See appendix A for details.

Products impacted by the change are:

EL4340IUZ EL4340IUZ-T13 EL4340IUZ-T7

**Reason for Change:**

The change in wafer fabrication site is necessary as the NXP facility in Fishkill, New York has discontinued manufacturing operations. The HS6 technology wafer fabrication process has been relocated from the NXP Fishkill to the NXP Nijmegen facility. The updated data sheet is available on the Intersil web site at: [EL4340 Datasheet](#)

**Product Identification:**

There will be no change in the external marking of the packaged parts. Product affected by this change is identifiable via Intersil's internal traceability system.

**Impact on fit, form, function, quality & reliability:**

The change will have no other impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

**Qualification status:** Complete, see Appendix B

**Sample availability:** 10/5/2017

**Device material declaration:** Available upon request

*Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.*

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: <a href="mailto:PCN-US@INTERSIL.COM">PCN-US@INTERSIL.COM</a>	Europe: <a href="mailto:PCN-EU@INTERSIL.COM">PCN-EU@INTERSIL.COM</a>	Japan: <a href="mailto:PCN-JP@INTERSIL.COM">PCN-JP@INTERSIL.COM</a>	Asia Pac: <a href="mailto:PCN-APAC@INTERSIL.COM">PCN-APAC@INTERSIL.COM</a>

Appendix A:

From:

**Electrical Specifications** V+ = +5V, V- = -5V, GND = 0V, TA = +25°C, Input Video = 1Vp-p and RL = 500Ω to GND, CL = 5pF unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>GENERAL</b>						
+I <sub>q</sub> Enabled	Enabled Supply Current (EL4340)	No load, V <sub>IN</sub> = 0V, Enable Low	26	30	34	mA
	Enabled Supply Current (EL4342)		39	46	50	mA
-I <sub>q</sub> Enabled	Enabled Supply Current (EL4340)	No load, V <sub>IN</sub> = 0V, Enable Low	-32	-30	-24	mA
	Enabled Supply Current (EL4342)		-48	-46	-36.5	mA
+I <sub>q</sub> Disabled	Disabled Supply Current (EL4340)	No load, V <sub>IN</sub> = 0V, Enable High	2.3	2.8	3.3	mA
	Disabled Supply Current (EL4342)	No load, V <sub>IN</sub> = 0V, Enable High	3	3.5	4	mA
-I <sub>q</sub> Disabled	Disabled Supply Current	No load, V <sub>IN</sub> = 0V, Enable High		10	100	μA
V <sub>OUT</sub>	Positive and Negative Output Swing	V <sub>IN</sub> = ±3.5V, R <sub>L</sub> = 500Ω	±3.1	±3.4		V
I <sub>OUT</sub>	Output Current	R <sub>L</sub> = 10Ω to GND	±80	±135		mA
V <sub>OS</sub>	Output Offset Voltage (EL4340)		-15	7	+15	mV
V <sub>OS</sub>	Output Offset Voltage (EL4342)		-10		+10	mV
I <sub>b</sub>	Input Bias Current	V <sub>IN</sub> = 0V	±1	-2	-3	μA
R <sub>OUT</sub>	HIZ Output Resistance	HIZ = Logic High		1.4		MΩ
R <sub>OUT</sub>	Enabled Output Resistance	HIZ = Logic Low		0.2		Ω
R <sub>IN</sub>	Input Resistance	V <sub>IN</sub> = ±3.5V		10		MΩ
A <sub>CL</sub> or A <sub>V</sub>	Voltage Gain	V <sub>IN</sub> = ±1.5V, R <sub>L</sub> = 500Ω	0.98	0.99	1.02	V/V
I <sub>TRI</sub>	Output Current in Three-state	V <sub>OUT</sub> = 0V	8	15	22	μA
<b>LOGIC</b>						
V <sub>IH</sub>	Input High Voltage (Logic Inputs)		2			V
V <sub>IL</sub>	Input Low Voltage (Logic Inputs)				0.8	V
I <sub>IH</sub>	Input High Current (Logic Inputs)	V <sub>IH</sub> = 5V	215	270	320	μA
I <sub>IL</sub>	Input Low Current (Logic Inputs)	V <sub>IL</sub> = 0V		2	3	μA

To:

**Electrical Specifications** V+ = +5V, V- = -5V, GND = 0V, TA = +25°C, Input Video = 1Vp-p and RL = 500Ω to GND, CL = 5pF unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>GENERAL</b>						
Enabled Supply current (EL4340)	+I <sub>q</sub> Enabled	No load, V <sub>IN</sub> = 0V, Enable Low	21.5	30	34	mA
Enabled Supply current (EL4342)			39	46	50	mA
Enabled Supply current (EL4340)	-I <sub>q</sub> Enabled	No load, V <sub>IN</sub> = 0V, Enable Low	-32	-30	-21	mA
Enabled Supply current (EL4342)			-48	-46	-36.5	mA
Disabled Supply current (EL4340)	+I <sub>q</sub> Disabled	No load, V <sub>IN</sub> = 0V, Enable High	1.75	2.8	4.2	mA
Disabled Supply current (EL4342)		No load, V <sub>IN</sub> = 0V, Enable High	3	3.5	4	mA
Disabled Supply current	-I <sub>q</sub> Disabled	No load, V <sub>IN</sub> = 0V, Enable High		10	100	μA
Positive and Negative Output Swing	V <sub>OUT</sub>	V <sub>IN</sub> = ±3.5V, R <sub>L</sub> = 500Ω	±3.1	±3.4		V
Output current	I <sub>OUT</sub>	R <sub>L</sub> = 10Ω to GND	±80	±135		mA
Output Offset Voltage (EL4340)	V <sub>OS</sub>		-15	7	+15	mV
Output Offset Voltage (EL4342)	V <sub>OS</sub>		-10		+10	mV
Input Bias current	I <sub>b</sub>	V <sub>IN</sub> = 0V	±0.5	-2	-3	μA
HIZ Output Resistance	R <sub>OUT</sub>	HIZ = Logic High		1.4		MΩ
Enabled Output Resistance	R <sub>OUT</sub>	HIZ = Logic Low		0.2		Ω
Input Resistance	R <sub>IN</sub>	V <sub>IN</sub> = ±3.5V		10		MΩ
Voltage Gain	A <sub>CL</sub> or A <sub>V</sub>	V <sub>IN</sub> = ±1.5V, R <sub>L</sub> = 500Ω	0.98	0.99	1.02	V/V
Output current in Three-State	I <sub>TRI</sub>	V <sub>OUT</sub> = 0V	8	15	22	μA
<b>LOGIC</b>						
Input High Voltage (Logic Inputs)	V <sub>IH</sub>		2			V
Input Low Voltage (Logic Inputs)	V <sub>IL</sub>				0.8	V
Input High current (Logic Inputs)	I <sub>IH</sub>	V <sub>IH</sub> = 5V	215	270	340	μA
Input Low current (Logic Inputs)	I <sub>IL</sub>	V <sub>IL</sub> = 0V		2	3	μA
<b>AC GENERAL</b>						
0.1% Settling Time	t <sub>s</sub>	Step = 1V		10		ns
Power Supply Rejection Ratio	PSRR (EL4340)	DC, PSRR V+ and V- combined	52	72		dB
Power Supply Rejection Ratio	PSRR (EL4342)	DC, PSRR V+ and V- combined	52	56		dB

**Appendix B: NXP HS6 Technology Qualification Summary**

Reliability Test	EL4543 NXP - HS6 Wafer Fabrication Process 24 Lead QSOP	ISL1557 NXP - HS6 Wafer Fabrication Process 16 LEAD 4X4 QFN
High Temperature Operating Life	0/240 125C for 2000 hours disposition = Passed	0/80 125C for 2000 hours disposition = Passed
High Temperature Storage	0/78 150C Bake and Reflow, 1000 hours disposition = Passed	N/A
Unbiased HAST	0/80 130C, 85%RH for 96 hours disposition = Passed	0/78 130C, 85%RH for 96 hours disposition = Passed
Biased HAST	0/158 130C, 85%RH for 96 hours disposition = Passed	N/A
Bond Pull Integrity	0/6 175C for 96hours disposition = Passed	0/3 175C for 96hours disposition = Passed
Temperature Cycle	0/80 -40C to 125C, 1000 cycles disposition = Passed	0/78 -40C to 125C, 1000 cycles disposition = Passed