REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

HSP50415EVAL1 SCHEMATICS

PAGE 1: TITLE
PAGE 2: HSP50415
PAGE 3: CPLD / SRAM
PAGE 4: POWER / MISC

DRAWN BY: STEVE HARRELL	DATE: 11/22/99	ENGINEER:	DATE:
RELEASED BY:	DATE:	TITLE: HSP50415EVAL1	
UPDATED BY:	DATE:		
intersil	TESTER	MASK# / HRDWR ID / REV. B2	
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REVISIONS				
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IOUT DATA

P3

IOUT<0..13>

HEADER MATES WITH HP16SXX LOGIC ANALYZER POD TERMINATION ADAPTER P/N 01650-63203

R69 OPEN

FOVRFL

CLKOUT

J6 (MMCX)

R70 34

VDD

DO<0..17>

J13

FLE-110

DIN14 DIN13 VDD GND DIN12 DIN11 DIN10 DIN9 DIN8 DIN7 DIN6 VDD DIN4 GND DIN3 DIN2 DIN1 DIN0 DATACLK

HSP50415VI

U4

DATACLK

J7 (MMCX)

CDATA<0..7>

J15

FLE-110

RD CE ADDR1 INTREQ RESETM

R65 34

REFCLK

SYMCLK2

J8 (MMCX)

C76 OPEN

R66 0

R3 1K

R4 1K

C3 0.1UF

R2 3K

U5 50330F OR GND HALF FULL

JP6

R5 49.9

J4 (SMA)

CLK INPUT

TP1 (BLACK)

C1 0.1UF C2 0.1UF

Y1 OSC PIN # 11 14

VCCA

C6 0.1UF C10 0.1UF

R8 2K

C7 0.1UF C11 0.1UF

JP5 EXT REF / INT EXT

R10 49.9 C37 10PF

R11 49.9 C38 10PF

R12 49.9 C41 10PF

R13 49.9 C44 10PF

R14 0 R15 0 R16 0 R17 0

R18 100 R19 100

R20 0 R21 0

T1 T1-1T

R1 OPEN R38 OPEN

J2 IOUT (SMA)

J3 QOUT (SMA)

TP13 (BLACK)

TP3 (WHITE)

TP4 (BLACK)

TP2 (BLACK)

REFERENCE (SMA)

R6 1.21K R7 OPEN R9 OPEN

C4 33PF C5 470PF C8 OPEN C9 OPEN

HSP50415 DECOUPLING CAPS WITH LOCATION REFERENCES

TOP LEFT	BOTTOM LEFT	PINS: 4	22	26	53	61	70	83	93	31	30	36	44	TOP RIGHT	BOTTOM RIGHT
VDD		VDD									VCCA			VCCA	
C72 1UF	C73 1UF	C12 0.1UF	C13 0.1UF	C23 0.1UF	C14 0.1UF	C16 0.1UF	C17 0.1UF	C18 0.1UF	C19 0.1UF	C24 0.1UF	C22 0.1UF	C20 0.1UF	C21 0.1UF	C74 1UF	C75 1UF
		C47 0.01UF	C50 0.01UF	C68 0.01UF	C51 0.01UF	C54 0.01UF	C64 0.01UF	C65 0.01UF	C66 0.01UF	C67 0.01UF	C69 0.01UF	C70 0.01UF	C71 0.01UF		

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

P5

JTAG HEADER

U2
CY37256V
208 PIN

U7
CY7C1327

U3
SN74ALVCH16823

DATA FLOPS

JS5

R71 3K
R72 3K
R73 3K
R74 3K
R75 3K

FFULL
FEMPTY
FOVRFL
LCKDET

LEDB<0..3>
LEDS<0..3>
DEBUG<0..15>
LED<0..19>
D<0..17>
A<0..19>
DQ<0..17>
CDATA<0..7>

TDI
TDO
TMS
TCK

WRITEB
DSTROBEB
RESETB
ASTROBEB
DB<0..7>
SPARE3B
INTRB
WAITB
SPARE1B
SPARE2B
HDB
DIR
PROGIMP
BADDR1
BADDR0
SYMD3
SYMD2
SYMD1
SYMD0

DATACLK
RCLKEN
RCLR
ROE
SYMCLK2
REFCLK

JP4
MANUAL DATACLK SELECT JUMPER
R68 34

C77 OPEN
R67 0
R23 1K
R24 1K
R22 3K
C25 0.1UF
JP7
R25 49.9
U5
SQ3300F OR GND
FULL HALF
J5
JS7

TP5 (BLACK)
TP6 (BLACK)

Y2 OSC
PIN # 11 14

FLOPS
PIN # 7 22 35 50

C30 0.1UF
C31 0.1UF

C32 C34 C35 C36 C40 C42 C45 C48 C52 0.1UF

CPLD
PIN # 26 52 78/80 104 130/132 156 182/184 207/208

C33 C35 C39 C43 C45 C49 C53 C55 0.1UF

SRAM
PIN # 4 11/15 20/27 41 54/61 65/70 77 91

C26 C27 C28 C29 0.1UF

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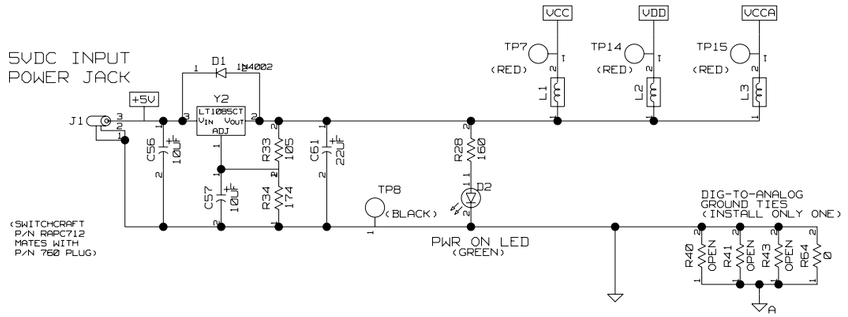
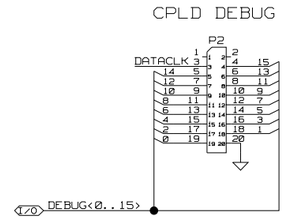
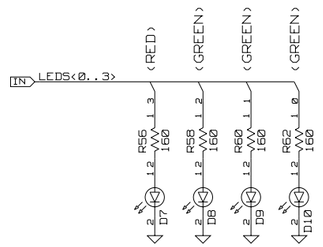
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

3.3VDC POWER DISTRIBUTION

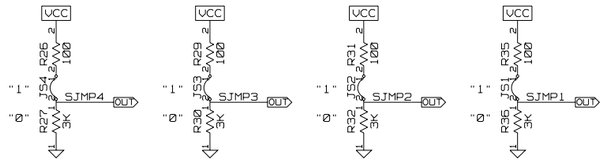


CPLD DEBUG

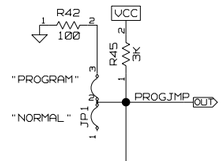




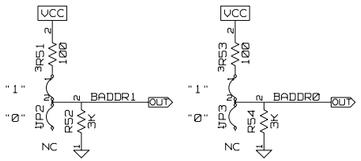
BOARD REVISION SOLDER JUMPERS



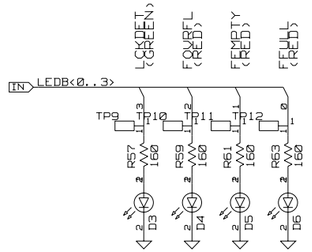
CPLD JTAG JUMPER



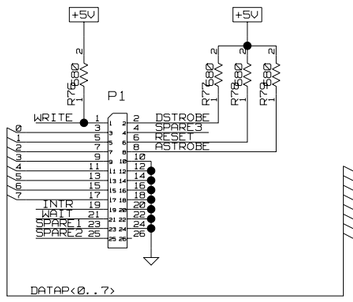
BOARD ADDRESS JUMPERS



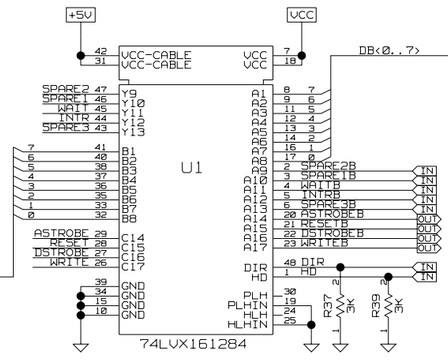
'415 STATUS LEDS



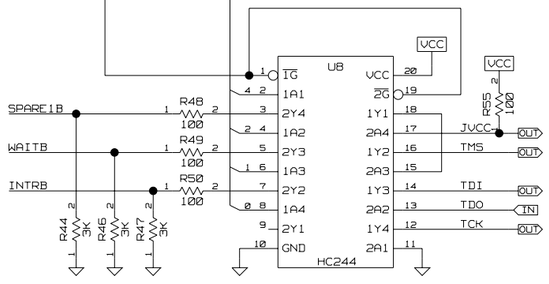
IDC26 PIN HEADER
(HOST PRN INTERFACE)



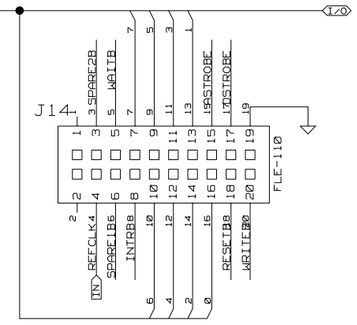
IEEE1284 TRANSCEIVER

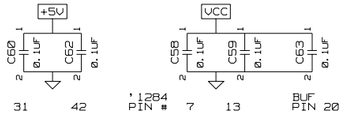


JTAG BUFFER



HOST DEBUG





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