Product Advisory (PA)

Subject: Datasheet endurance and electrical characteristics for High Performance Serial MRAM Memory datasheet
Publication Date: 3/1/2021
Effective Date: 3/1/2021

Revision Description:
Initial Release

Description of Change:
This notice is to inform you that the High Performance Serial MRAM Memory datasheet has been updated as follows;
Electrical Characteristics Section
Endurance has been changed from 10^{16} to 10^{14} cycles.
Various changes to the electrical currents.

Changes are reflected in Appendix A of the notice.

Affected Product List:
Please refer to Appendix B

Reason for Change:
[1] We have chosen to represent endurance with a conservative linear model resulting in our choice of 10^{14} cycles. The previous value 10^{16} represented a power law model for oxide reliability.
[2] We have modified the currents in the electrical characteristics tables to reflect long-term variation of the data.

Impact on Fit, Form, Function, Quality & Reliability:
No impact on Fit, Form, Function and Quality. Reliability of the device has not changed. We have chosen a more conservative model for endurance cycles and updated currents to reflect long term variability.

Product Identification:
Not Applicable

Qualification Status: Not Applicable, correction only
Sample Availability Date: 3/1/2021
Device Material Declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Renesas within 30 days of the publication date.

For additional information regarding this notice, please contact idt-pcn@lm.renesas.com

Appendix A - Description of Change

1. Configuration Register 2 (Read/Write) (Section 12.7, Table 22)

Table 22: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

FROM:

Table 22: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

Read Type	Latency	Max Frequency	
		Mxxxx2x108xx	Mxxxx2x054xx
(1-1-1) SDR	8-15	108MHz	54MHz
(1-1-1) DDR	8-15	54MHz	27MHz
(1-1-2) SDR	8-15	108MHz	54MHz
(1-2-2) SDR	8-15	108MHz	54MHz
(2-2-2) SDR	8-15	108MHz	54MHz
(2-2-2) DDR	8-15	54MHz	27MHz
(1-1-4) SDR	8-15	108MHz	54MHz
(1-4-4) SDR	8-15	108MHz	54MHz
(1-4-4) DDR	8-15	54MHz	27MHz
(4-4-4) SDR	12-15	108MHz	
	8-15		54MHz
(4-4-4) DDR	8-15	54MHz	27MHz

TO:

Table 22: Memory Array Read Latency Cycles vs. Maximum Clock Frequency (with XIP)

Read Type	Latency	Max Frequency	
		Mxxxx2x108xx	Mxxxx2x054xx
(1-1-1) SDR	8-15	108MHz	54MHz
(1-1-1) DDR		54MHz	27MHz
(1-1-2) SDR		108MHz	54MHz
(1-2-2) SDR		108MHz	54MHz
(2-2-2) SDR		108MHz	54MHz
(2-2-2) DDR		54MHz	27MHz
(1-1-4) SDR	12-15	108MHz	54MHz
(1-4-4) SDR		108MHz	54MHz
(1-4-4) DDR		54MHz	27MHz
(4-4-4) SDR		108MHz	
			54MHz
(4-4-4) DDR		54MHz	27MHz

2. Electrical Specifications (Section 15, Table 31, Table 32, Table 33):

a. Table 31: Endurance & Retention

FROM:

Table 31: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	85°C	20	years

TO:

Table 31: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{14}	cycles
Data Retention	RET	105°C	10	years
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

b. Table 32: 3.0V DC Characteristics

FROM:

Table 32: 3.0V DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			Units
				Minimum	Typical	Maximum	
Read Current (1-1-1) SDR	I_{READ1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	8	9	mA
Read Current (2-2-2) SDR	I_{READ2}			-	9	10	mA
Read Current (4-4-4) SDR	I_{READ3}			-	10	12	mA
Read Current (1-1-1) SDR	I_{READ4}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	13	14	mA
Read Current (2-2-2) SDR	I_{READ5}			-	15	15	mA
Read Current (4-4-4) SDR	I_{READ6}			-	19	21	mA
Read Current (1-1-1) DDR	I_{READ7}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	9	10	mA
Read Current (2-2-2) DDR	I_{READ8}			-	10	11	mA
Read Current (4-4-4) DDR	I_{READ9}			-	12	13	mA
Write Current (1-1-1) SDR	I_{WRITE1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	14	15	mA
Write Current (2-2-2) SDR	I_{WRITE2}			-	15	20	mA
Write Current (4-4-4) SDR	I_{WRITE3}			-	22	25	mA
Write Current (1-1-1) SDR	I_{WRITE4}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	22	25	mA
Write Current (2-2-2) SDR	I_{WRITE5}			-	25	30	mA
Write Current (4-4-4) SDR	I_{WRITE6}			-	38	40	mA
Write Current (1-1-1) DDR	I_{WRITE7}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	15	20	mA
Write Current (2-2-2) DDR	I_{WRITE8}			-	20	25	mA
Write Current (4-4-4) DDR	I_{WRITE9}			-	30	35	mA
Standby Current	I_{SB}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	160	-	µA
			Ta = 85ºC	-	-	400	µA
			Ta =105ºC	-	-	600	µA
Deep Power Down Current	I_{DPD}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	1.2	10	µA
Hibernate Current	I_{HBN}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	0.1	-	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA		V_{CC}-0.2	-	-	V
		I_{OH} = -1mA		2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA		-	-	0.2	V
		I_{OL} = 2mA		-	-	0.4	V

TO:

Table 32: 3.0V DC Characteristics

Parameter	Symbol	Test Conditions		3.0V Device (2.7V-3.6V)			Units
				Minimum	Typical	Maximum	
Read Current (1-1-1) SDR	I_{READ1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	8	9	mA
Read Current (2-2-2) SDR	I_{READ2}			-	9	10	mA
Read Current (4-4-4) SDR	I_{READ3}			-	10	12	mA
Read Current (1-1-1) SDR	I_{READ4}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	13	15	mA
Read Current (2-2-2) SDR	I_{READ5}			-	15	17	mA
Read Current (4-4-4) SDR	I_{READ6}			-	19	21	mA
Read Current (1-1-1) DDR	I_{READ7}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	13	18	mA
Read Current (2-2-2) DDR	I_{READ8}			-	20	24	mA
Read Current (4-4-4) DDR	I_{READ9}			-	23	28	mA
Write Current (1-1-1) SDR	I_{WRITE1}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	14	16	mA
Write Current (2-2-2) SDR	I_{WRITE2}			-	17	20	mA
Write Current (4-4-4) SDR	I_{WRITE3}			-	22	25	mA
Write Current (1-1-1) SDR	I_{WRITE4}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	22	28	mA
Write Current (2-2-2) SDR	I_{WRITE5}			-	25	32	mA
Write Current (4-4-4) SDR	I_{WRITE6}			-	38	45	mA
Write Current (1-1-1) DDR	I_{WRITE7}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	15	25	mA
Write Current (2-2-2) DDR	I_{WRITE8}			-	20	30	mA
Write Current (4-4-4) DDR	I_{WRITE9}			-	30	45	mA
Standby Current	I_{SB}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	160	-	µA
			Ta = 85ºC	-	-	400	µA
			Ta =105ºC	-	-	600	µA
Deep Power Down Current	I_{DPD}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	5	25	µA
Hibernate Current	I_{HBN}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	0.1	-	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA		V_{CC}-0.2	-	-	V
		I_{OH} = -1mA		2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA		-	-	0.2	V
		I_{OL} = 2mA		-	-	0.4	V

c. Table 33: 1.8V DC Characteristics

FROM:

Table 33: 1.8V DC Characteristics

Parameter	Symbol	Test Conditions		1.8V Device (1.71V-2.0V)			Units
				Minimum	Typical	Maximum	
Read Current (1-1-1) SDR	I_{READ1}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	7	8	mA
Read Current (2-2-2) SDR	I_{READ2}			-	7	8	mA
Read Current (4-4-4) SDR	I_{READ3}			-	8	9	mA
Read Current (1-1-1) SDR	I_{READ4}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	10	11	mA
Read Current (2-2-2) SDR	I_{READ5}			-	12	13	mA
Read Current (4-4-4) SDR	I_{READ6}			-	13	15	mA
Read Current (1-1-1) DDR	I_{READ7}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	7	8	mA
Read Current (2-2-2) DDR	I_{READ8}			-	8	10	mA
Read Current (4-4-4) DDR	I_{READ9}			-	8	10	mA
Write Current (1-1-1) SDR	I_{WRITE1}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	10	13	mA
Write Current (2-2-2) SDR	I_{WRITE2}			-	13	15	mA
Write Current (4-4-4) SDR	I_{WRITE3}			-	19	25	mA
Write Current (1-1-1) SDR	I_{WRITE4}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	17	22	mA
Write Current (2-2-2) SDR	I_{WRITE5}			-	22	25	mA
Write Current (4-4-4) SDR	I_{WRITE6}			-	32	38	mA
Write Current (1-1-1) DDR	I_{WRITE7}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	14	15	mA
Write Current (2-2-2) DDR	I_{WRITE8}			-	18	20	mA
Write Current (4-4-4) DDR	I_{WRITE9}			-	28	30	mA
Standby Current	I_{SB}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	120	-	µA
			Ta = 85ºC	-	-	350	µA
			Ta=105ºC	-	-	500	µA
Deep Power Down Current	I_{DPD}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	1	10	µA
Hibernate Current	I_{HBN}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	0.1	-	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
WP# Leakage Current	$I_{WP\#LI}$	V_{IN}=0 to V_{CC} (max)		-100.0	-	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA		V_{CC}-0.2	-	-	V
		I_{OH} = -1mA		1.5	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA		-	-	0.2	V
		I_{OL} = 2mA		-	-	0.4	V

TO:

Table 33: 1.8V DC Characteristics

Parameter	Symbol	Test Conditions		1.8V Device (1.71V-2.0V)			Units
				Minimum	Typical	Maximum	
Read Current (1-1-1) SDR	I_{READ1}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	5	8	mA
Read Current (2-2-2) SDR	I_{READ2}			-	6	9	mA
Read Current (4-4-4) SDR	I_{READ3}			-	7	11	mA
Read Current (1-1-1) SDR	I_{READ4}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	8	12	mA
Read Current (2-2-2) SDR	I_{READ5}			-	9	13	mA
Read Current (4-4-4) SDR	I_{READ6}			-	12	17	mA
Read Current (1-1-1) DDR	I_{READ7}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	11	14	mA
Read Current (2-2-2) DDR	I_{READ8}			-	17	20	mA
Read Current (4-4-4) DDR	I_{READ9}			-	21	25	mA
Write Current (1-1-1) SDR	I_{WRITE1}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	13	15	mA
Write Current (2-2-2) SDR	I_{WRITE2}			-	16	19	mA
Write Current (4-4-4) SDR	I_{WRITE3}			-	20	23	mA
Write Current (1-1-1) SDR	I_{WRITE4}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=108MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	20	26	mA
Write Current (2-2-2) SDR	I_{WRITE5}			-	23	30	mA
Write Current (4-4-4) SDR	I_{WRITE6}			-	36	43	mA
Write Current (1-1-1) DDR	I_{WRITE7}	V_{CC} = 2.0V, I_{OUT}=0mA, CLK=54MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}		-	13	23	mA
Write Current (2-2-2) DDR	I_{WRITE8}			-	19	28	mA
Write Current (4-4-4) DDR	I_{WRITE9}			-	28	43	mA
Standby Current	I_{SB}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}	Ta = 25ºC	-	140	-	µA
			Ta = 85ºC	-	-	350	µA
			Ta=105ºC	-	-	500	µA
Deep Power Down Current	I_{DPD}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	4	20	µA
Hibernate Current	I_{HBN}	V_{CC} = 2.0V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}		-	0.1	-	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)		-	-	±1.0	µA
WP# Leakage Current	$I_{WP\#LI}$	V_{IN}=0 to V_{CC} (max)		-100.0	-	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)		-	-	±1.0	µA
Input High Voltage	V_{IH}			0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA		V_{CC}-0.2	-	-	V
		I_{OH} = -1mA		1.5	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 150µA		-	-	0.2	V
		I_{OL} = 2mA		-	-	0.4	V

3. CS# Operation & Timing (Section 15.1, Table 36)

Table 36: CS# Operation

FROM:

Table 36: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	108 (SDR)	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Register Write Cycle[1]	t_{CS2}	5	-	µs
Chip Deselect Time after Write Cycle (SPI)	t_{CS3}	250	-	ns
Chip Deselect Time after Write Cycle (DPI)	t_{CS4}	320	-	ns
Chip Deselect Time after Write Cycle (QPI)	t_{CS5}	420[2]	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:
Power supplies must be stable
1:SDR operation only
2:For single byte operations, t_{CS5} is 230ns

TO:

Table 36: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1	108 (SDR)	MHz
Clock Low Time	t_{CL}	0.45 * 1/ f_{CLK}	-	ns
Clock High Time	t_{CH}	0.45 * 1/ f_{CLK}	-	ns
Chip Deselect Time after Read Cycle	t_{CS1}	20	-	ns
Chip Deselect Time after Register Write Cycle[1]	t_{CS2}	5	-	µs
Chip Deselect Time after Write Cycle (SPI)	t_{CS3}	280	-	ns
Chip Deselect Time after Write Cycle (DPI)	t_{CS4}	350	-	ns
Chip Deselect Time after Write Cycle (QPI)	t_{CS5}	490[2]	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	4	-	ns

Notes:
Power supplies must be stable
1:SDR operation only
2:For single byte operations, t_{CS5} is 280ns

Appendix B - Affected Product List

Part Numbers		
M10042040108X0IWAR	M10162040108X0IWAR	M10082040054X0IWAR
M10042040108X0IWAY	M10162040108X0IWAY	M10082040054X0IWAY
M10042040108X0ISAR	M10162040108X0ISAR	M10082040054X0ISAR
M10042040108X0ISAY	M10162040108X0ISAY	M10082040054X0ISAY
M10042040108X0PWAR	M10162040108X0PWAR	M10082040054X0PWAR
M10042040108X0PWAY	M10162040108X0PWAY	M10082040054X0PWAY
M10042040108X0PSAR	M10162040108X0PSAR	M10082040054X0PSAR
M10042040108X0PSAY	M10162040108X0PSAY	M10082040054X0PSAY
M30042040108X0IWAR	M30162040108X0IWAR	M30082040054X0IWAR
M30042040108X0IWAY	M30162040108X0IWAY	M30082040054X0IWAY
M30042040108X0ISAR	M30162040108X0ISAR	M30082040054X0ISAR
M30042040108X0ISAY	M30162040108X0ISAY	M30082040054X0ISAY
M30042040108X0PWAR	M30162040108X0PWAR	M30082040054X0PWAR
M30042040108X0PWAY	M30162040108X0PWAY	M30082040054X0PWAY
M30042040108X0PSAR	M30162040108X0PSAR	M30082040054X0PSAR
M30042040108X0PSAY	M30162040108X0PSAY	M30082040054X0PSAY
M10082040108X0IWAR	M10042040054X0IWAR	M10162040054X0IWAR
M10082040108X0IWAY	M10042040054X0IWAY	M10162040054X0IWAY
M10082040108X0ISAR	M10042040054X0ISAR	M10162040054X0ISAR
M10082040108X0ISAY	M10042040054X0ISAY	M10162040054X0ISAY
M10082040108X0PWAR	M10042040054X0PWAR	M10162040054X0PWAR
M10082040108X0PWAY	M10042040054X0PWAY	M10162040054X0PWAY
M10082040108X0PSAR	M10042040054X0PSAR	M10162040054X0PSAR
M10082040108X0PSAY	M10042040054X0PSAY	M10162040054X0PSAY
M30082040108X0IWAR	M30042040054X0IWAR	M30162040054X0IWAR
M30082040108X0IWAY	M30042040054X0IWAY	M30162040054X0IWAY
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M30082040108X0PWAR	M30042040054X0PWAR	M30162040054X0PWAR
M30082040108X0PWAY	M30042040054X0PWAY	M30162040054X0PWAY
M30082040108X0PSAR	M30042040054X0PSAR	M30162040054X0PSAR
M30082040108X0PSAY	M30042040054X0PSAY	M30162040054X0PSAY