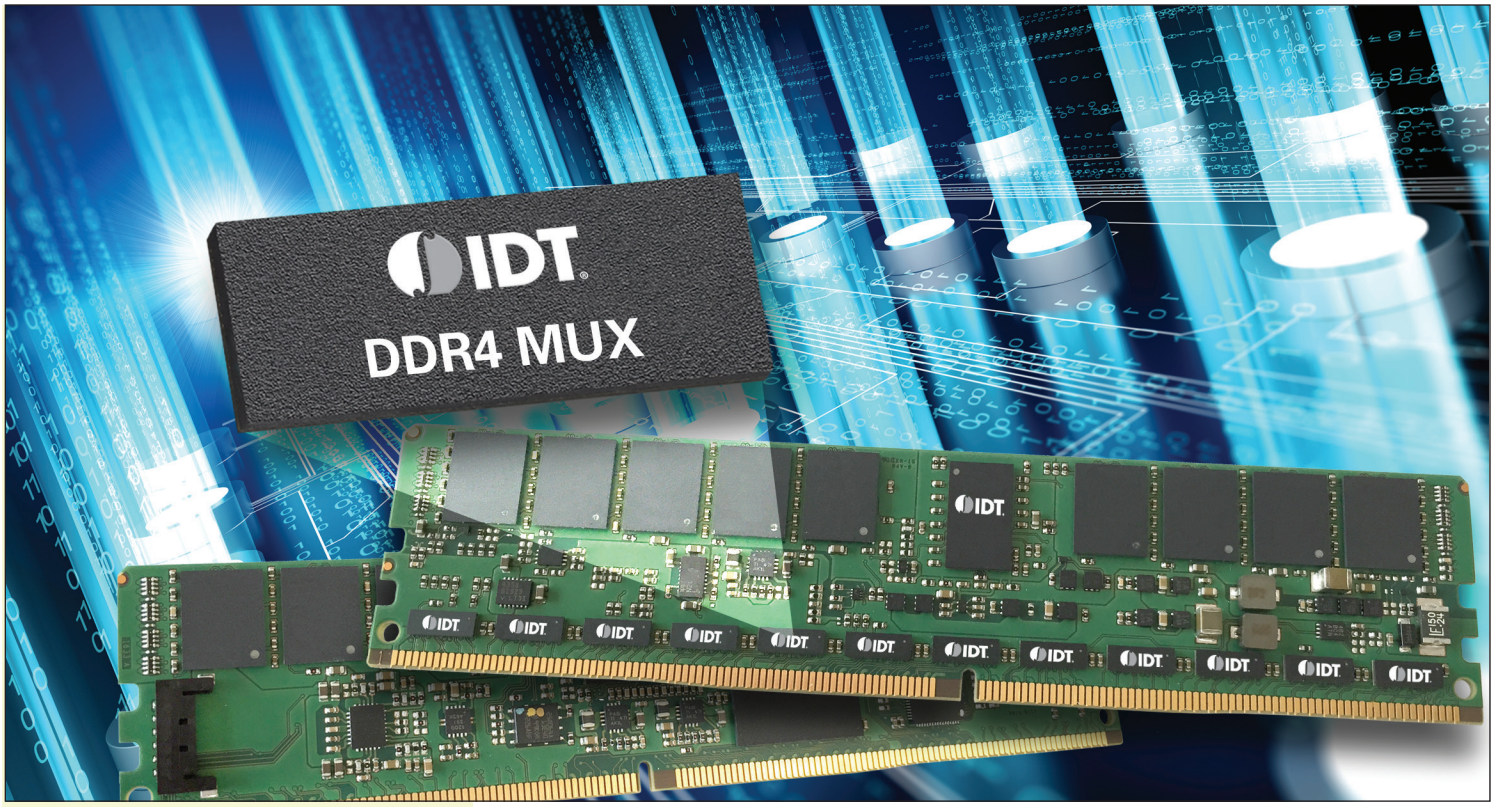
Integrated Device Technology

4MX0121V Switch/Multiplexer for DDR3/DDR4 NVDIMM

CLOCKS AND TIMING | INTERFACE AND CONNECTIVITY | **MEMORY AND LOGIC** | POWER MANAGEMENT | RF PRODUCTS



FEATURES AND BENEFITS

- Host controller bus isolation from the DRAM memory during NVDIMM "save" and "restore" operations between DRAM and non-volatile memory
- AC and DC parameters optimized for DDR4, enabling the highest possible memory channel performance for NVDIMMs even when intermixed with other DIMM types
- 12-bit bus switch/multiplexer to best match the eight DQ pins and four DQS pins from each DRAM
- Make-before-break circuit to prevent glitches during switching operations
- Simple CMOS select and enable pins (SEL0, SEL1, EN)
- Available in a 3 x 8 mm 48-ball VFBGA package with 0.65 mm ball pitch that can replace data buffers on the DIMM for NVDIMM applications

APPLICATIONS

- DDR4 NVDIMM
- DDR3 NVDIMM

The 4MX0121V is a 12-bit bus switch/multiplexer designed for 2.5 V or 3.3 V supply voltage operation in DDR3 and DDR4 memory bus systems.

The device has a 1:2 switch or 2:1 multiplex topology. Each 12-bit wide A-port can be switched to one of two ports B and C, for all bits simultaneously. Each port is bidirectional for high-speed and high-bandwidth switch multiplexer applications. Port selection uses two simple input selection pins and all ports can be disconnected via an enable pin. The device is divided into two 6-bit bus switch/multiplexers for additional flexibility.

The 4MX0121V uses a high-speed switch architecture providing high bandwidth, low insertion loss, low return loss, and very low propagation delay, allowing use in many applications requiring switching or multiplexing of high-speed signals. It is available in a 3 x 8 mm 48-ball VFBGA package with 0.65 mm ball pitch for optimal size versus board layout density.

Discover what IDT know-how can do for you:
IDT.com/go/DDR4 | IDT.com/go/DDR3

PB_NVDIMM-MUX_REVA0315