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Key Features of Renesas Electronics' New EMMA™3SE/P and EMMA3SL2/LP

Integrated DVB-T/C demodulator

DVB-T ETS 300-744 compliant
DVB-C ETS 300-429 compliant

On-chip CPU

Main CPU:
MIPS32® 4KEc® core
Sub CPU:
MIPS32 4KEc core

Memory Interface

DDR3: 1333 MHz, 16-bit bus, Supports up to 512 MB memory
Supports NOR, NAND and serial flash ROM
Up to 256 Gb NAND

MPEG Transport Stream Processing Engine

Supports three transport stream inputs
MPEG2 TS

Video Decoder

MPEG2 MP@HL (EMMA3SE/P), MP@ML (EMMA3SL2/LP)
MPEG4 AVC: HP@L4.2 (EMMA3SE/P), HP@L3.0 (EMMA3SL2/LP)
MPEG4 MVC: Stereo HP@L4.1
VP6, Sorenson Spark

Audio Controller

MPEG1 / MPEG2 layer 1 or 2, MP3
MPEG2 AAC, MPEG4 AAC, HE-AAC V1 L2/L4, V2 L2/L4
Dolby® Digital, Dolby Digital Plus, MS10
DTS®
SPDIF output

Display and Graphics

Video 2 planes, OSD 2 planes, background 1 plane
Sub display 2 planes

Peripherals support

SATA - 1 channel
HDMI output - 1 channel
USB 2.0 host controller - 2 channels
Ethernet controller - 1 channel
Two UARTs
Two smart card interfaces
Two I2C interfaces
IR receiver, timer

Package

336-pin, 0.8 mm pitch, 17 mm × 17 mm FPBGA (Fine Pitch Plastic Ball Grid Array)