September 26, 2013

Product Specifications of the R-Car M2

Item	Specification	
Product number	R8A7791	
Power supply voltage	3.3/1.8 V (IO), 1.5/1.35 V (DDR3), 1.03 V (Core)	
CPU core	ARM®Cortex™-A15 Dual	SH-4A core (device option)
Maximum operating frequency	1.5 GHz	780 MHz
Processing performance	10500 DMIPS	1720 DMIPS
Cache memory	L1 Instruction cache: 32 KB L1 Operand cache: 32 KB L2 Cache: 2 MB	Instruction cache: 32 KB Operand cache: 32 KB
External memory	DDR3-SDRAM Maximum operating frequency: 800 MHz Data bus width: 32 bits × 2 ch (6.4 GB/s × 2)	
Expansion bus	Flash ROM and SRAM, Data bus width: 8 or 16 bits	
	PCI Express2.0 (1 lane)	
Graphics	PowerVR SGX 544MP2 (3D)	
	Renesas graphics processor (2D)	
Video	Display Out × 2 ch (1 ch: LVDS, 1 ch: RGB888)	
	Video Input × 3 ch	
	Video codec module (H.264/AVC, MPEG-2/4, VC-1)	
	IP conversion module	

Item	Specification
	JPEG accelerator
	TS Interface × 1 ch
	Video image processing (color conversion, image expansion, reduction, filter processing)
	Distortion compensation module (image renderer) × 1 ch
Audio	Audio DSP
	Sampling rate converter × 10 ch
	Serial sound interface × 10 ch
	MOST DTCP
Storage Interface	USB 3.0 host interface × 1 port (wPHY)
	USB 2.0 host interface × 2 ports (wPHY)
	SD host interface × 3 ch (SDXC, UHS-I)
	Multimedia card interface × 1 ch
	Serial ATA interface × 2 ch
In-car network and automotive peripherals	Media local bus (MLB) Interface × 1 ch (6-pin / 3-pin interface selectable)
	CAN Interface × 2 ch
	IEBus™ Interface
	GPS baseband module (Galileo, GLONASS) (device option)
	Ethernet controller AVB (IEEE802.1BA, 802.1AS, 802.1Qav and IEEE1722, GMII/MII, without PHY)
Security	Crypto engine (AES, DES, Hash, RSA)
	Secure RAM
Other peripherals	DMA controller LBSC DMAC: 3 ch / SYS-DMAC : 30 ch / RT-DMAC: 3 ch / Audio-DMAC: 26 ch / Audio (peripheral)-DMAC: 29 ch
	32 bit timer × 12 ch
	PWM timer × 7 ch
	I^2C bus interface × 9 ch
	Serial communication interface (SCIF) × 18 ch

Item	Specification
	Quad serial peripheral interface (QSPI) × 1 ch (for boot)
	Clock-synchronized serial interface (MSIOF) × 3 ch (SPI/IIS)
	Ethernet AVB controller (IEEE802.1BA/802.1AS/802.1Qav/IEEE1722, GMII/MII, without PHY)
	Ethernet controller (IEEE802.3u, RMII, without PHY)
	Interrupt controller (INTC)
	Clock generator (CPG) with built-in PLL
	On-chip debugger interface
Low power mode	Dynamic Power Shutdown (CPU core, 3D, IMP) AVS and DVFS function DDR-SDRAM power supply backup mode
Package	831-pin Flip Chip BGA (27 mm × 27 mm)

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