# ISL72991RH

Low Dose Rate Total Dose Testing of the ISL72991RH Negative Voltage Regulator

## Introduction

This report provides results of a Low Dose Rate (LDR) total ionizing dose (TID) test of the ISL72991RH radiation hardened negative linear voltage regulator. The test was conducted in order to determine the sensitivity of the part to LDR irradiation. The ISL72991RH does not have a corresponding -EH version and is lot acceptance tested (RLAT) at High Dose Rate (HDR) only. The present limited LDR data is for biased irradiation only and was developed in 2008; it is provided for guidance only as the part is not specified for LDR performance. The dose rate used for this test was 0.01rad(Si)/s.

## Related Information

- MIL-STD-883 test method 1019
- ISL72991RH datasheet
- DLA Standard Microcircuit Drawing (SMD) 5962-02503

# Contents




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# 1. Product Description

The radiation hardened ISL72991RH is a low dropout adjustable negative linear regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM), and a shutdown pin (SD) for easy on/off control. The ISL72991RH incorporates unique circuitry that enables precision performance across the -55°C to +125°C temperature range and post-irradiation. Datasheet specifications across the full temperature range include an internal reference voltage of -1.25V +40mV/-50mV (maximum), line regulation of ±25mV (maximum), and load regulation of ±15mV (maximum). The reference voltage is the ADJ pin to GND voltage. Figure 1 shows a functional diagram.

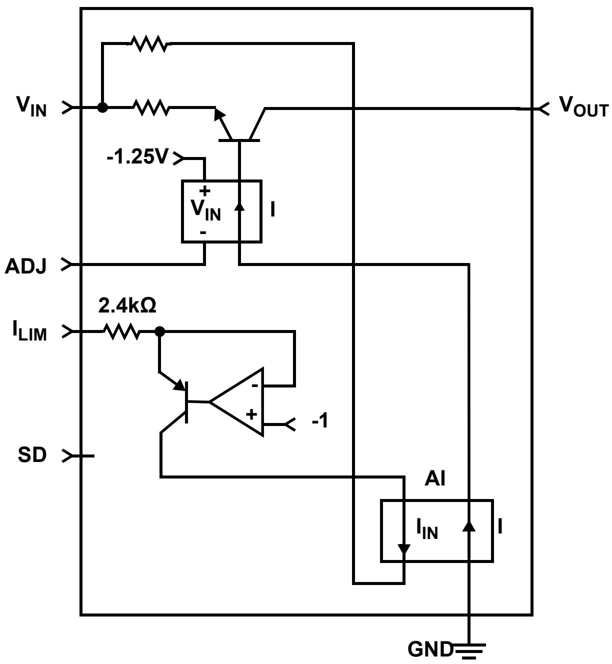


**Figure 1. ISL72991RH Functional Diagram**

Constructed with the dielectrically isolated Radiation Hardened Silicon Gate (RSG) BiCMOS process, the device is immune to single event latch-up and has been specifically designed to provide highly reliable performance in harsh radiation environments. The part is fully specified in Standard Microcircuit Drawing 5962-02503, which is the controlling document. The ISL72991RH is available in a 28 Ld hermetic ceramic flatpack or in die form and is specified across the military temperature range of -55°C to +125°C.

# 2. Test Description

## 2.1 Irradiation Facilities

LDR testing used a J. L. Shepherd and Associates model 484 LDR located in the Renesas Palm Bay, FL facility. The irradiations were performed at 0.010rad(Si)/s per MIL-STD-883 Method 1019. Because of the capacity limitations of the Model 484 irradiator only biased irradiation was performed.

## 2.2 Test Fixturing

The irradiation bias circuit was a standard low power dissipation back bias configuration.

## 2.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using production automated test equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature only.

## 2.4 Experimental Matrix

Testing proceeded in accordance with MIL-STD-883 Test Method 1019. The experimental matrix consisted of 13 samples irradiated at LDR under bias. Samples of the ISL72991RH were packaged in production 28 Ld ceramic flatpacks.

## 2.5 Downpoints

The downpoints for the test were 0krad(Si), 10krad(Si), 25krad(Si), and 85krad(Si).

# 3. Results

LDR total dose testing of the ISL72991RH showed no reject devices to the SMD post-radiation limits after 85krad(Si). All parameters showed good stability.

## 3.1 Attributes Data

**Table 1. Attributes Data**

| Part | Dose Rate (rad(Si)/s) | Bias | Sample Size | Downpoint | Pass[1] | Fail |
|---|---|---|---|---|---|---|
| ISL72991RH | 0.01 | Biased | 13 | Pre-irradiation | | |
| | | | | 10krad(Si) | 13 | 0 |
| | | | | 25krad(Si) | 13 | 0 |
| | | | | 85krad(Si) | 13 | 0 |

1. A Pass indicates a sample that passes all SMD 5962-02503 limits.

## 3.2 Variables Data

Figure 2 through Figure 10 show the total dose response of selected parameters at all downpoints. The plots show the average as a function of total dose.

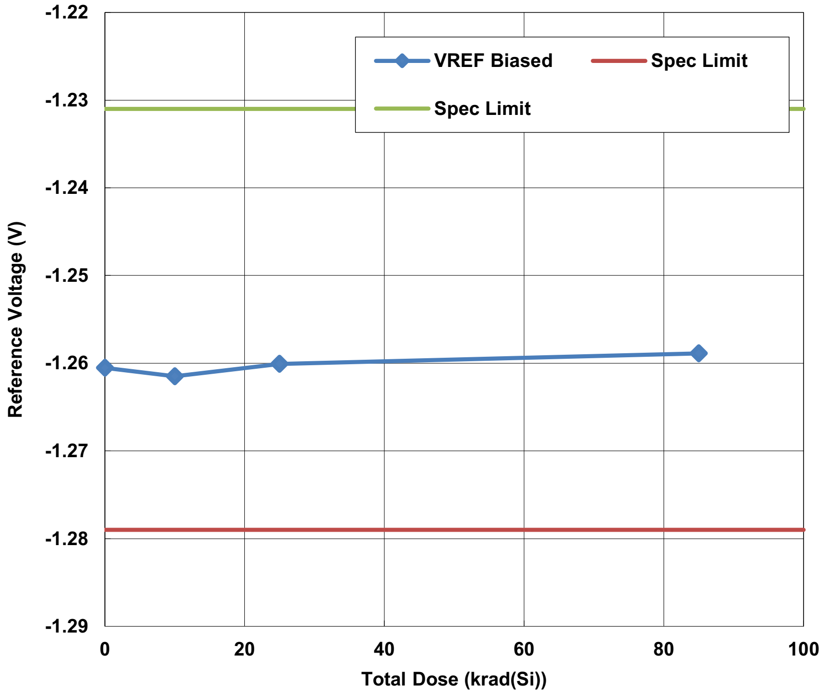


**Figure 2. ISL72991RH negative voltage regulator reference voltage as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limit is -1.279V to -1.231V.**

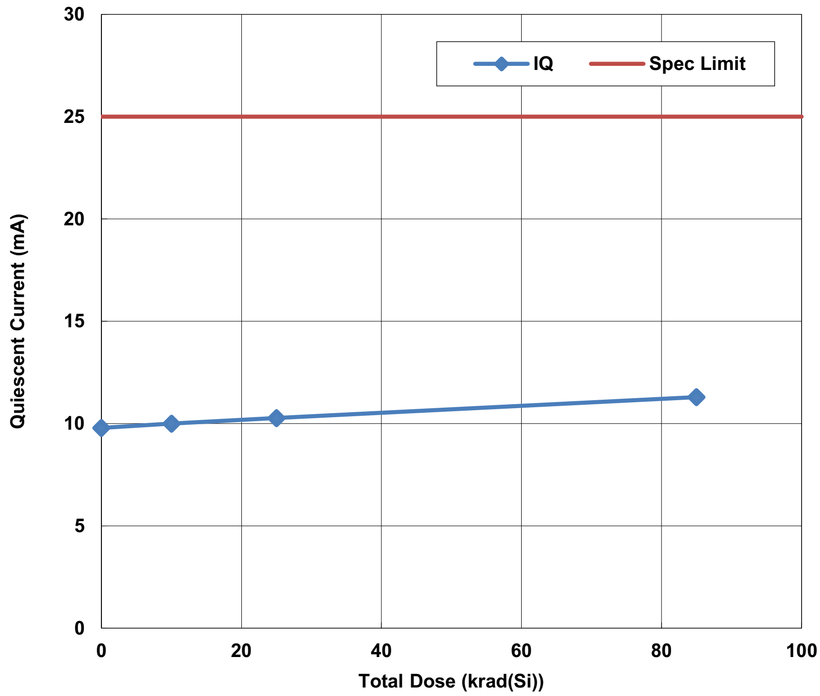


**Figure 3. ISL72991RH negative voltage regulator quiescent current at dropout as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limit is 25mA maximum.**

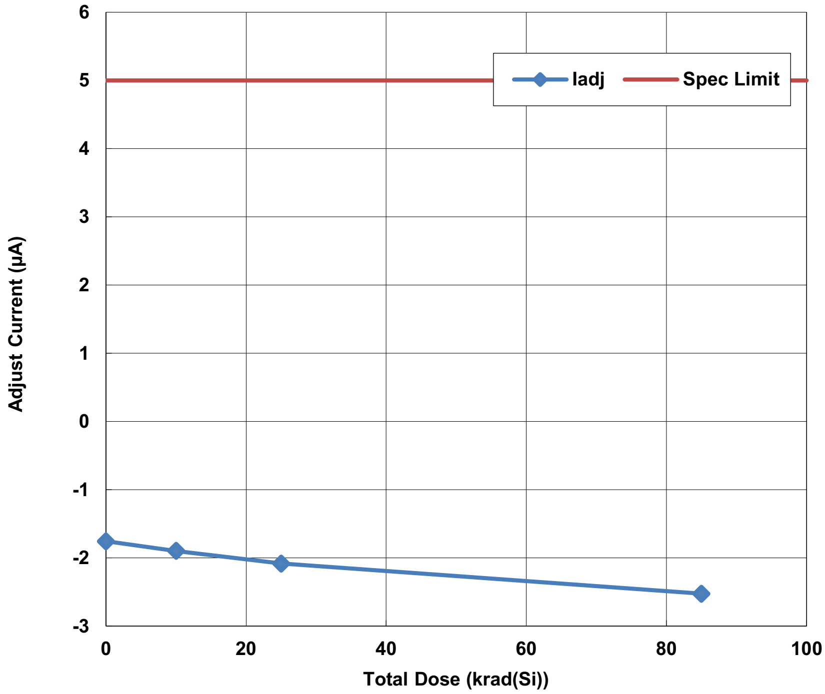


**Figure 4. ISL72991RH negative voltage regulator adjust current as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limit is 5µA maximum; internal ATE limits are -5µA to 5µA.**

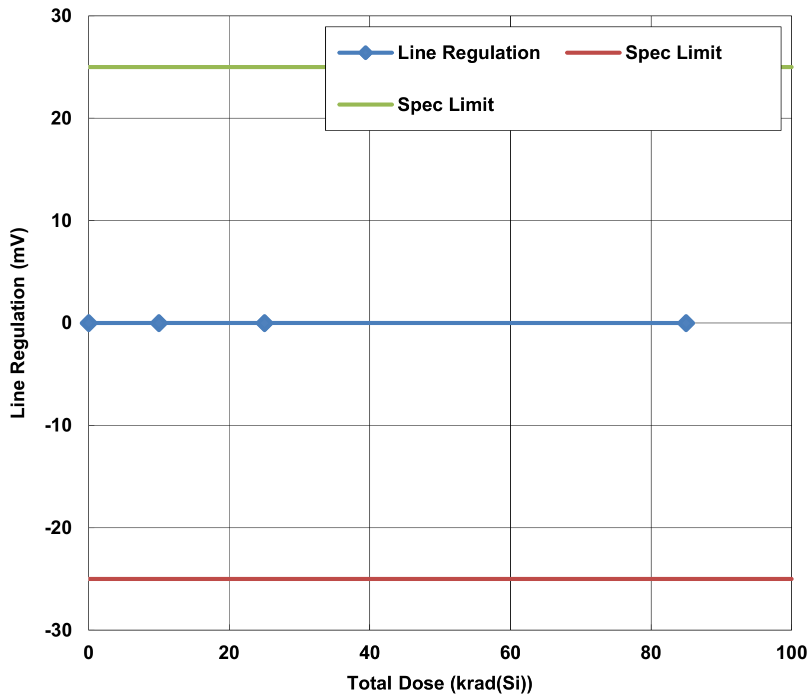


**Figure 5. ISL72991RH negative voltage regulator line regulation as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limits are -25mV to 25mV.**

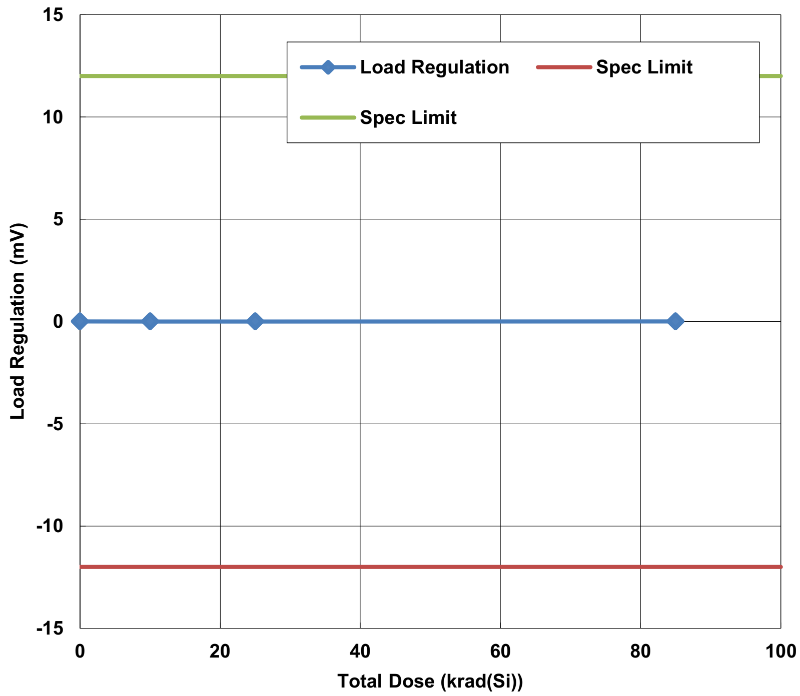


**Figure 6. ISL72991RH negative voltage regulator load regulation as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limits are -12mV to 12mV.**

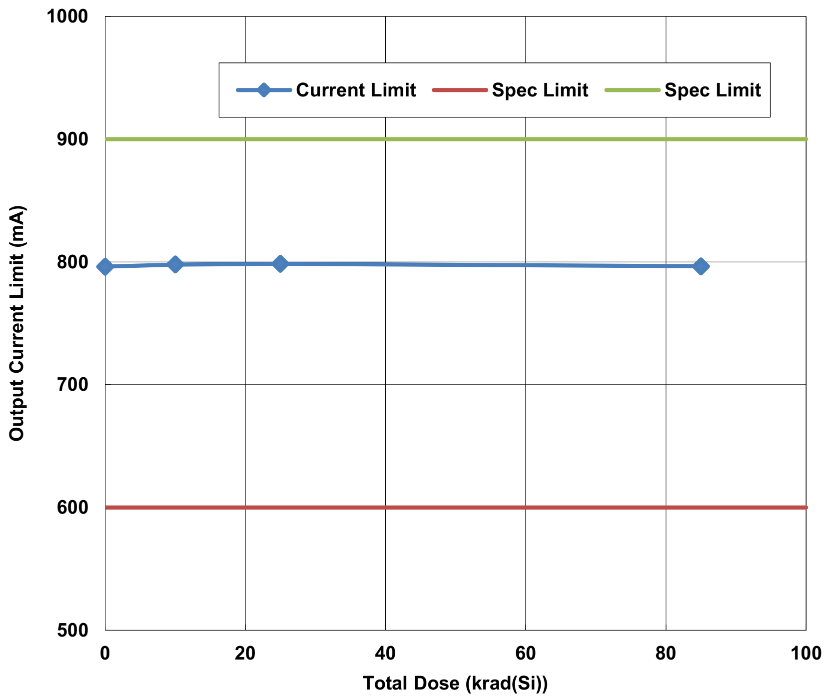


**Figure 7. ISL72991RH negative voltage regulator output current limit as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limits are 600mA to 900mA.**

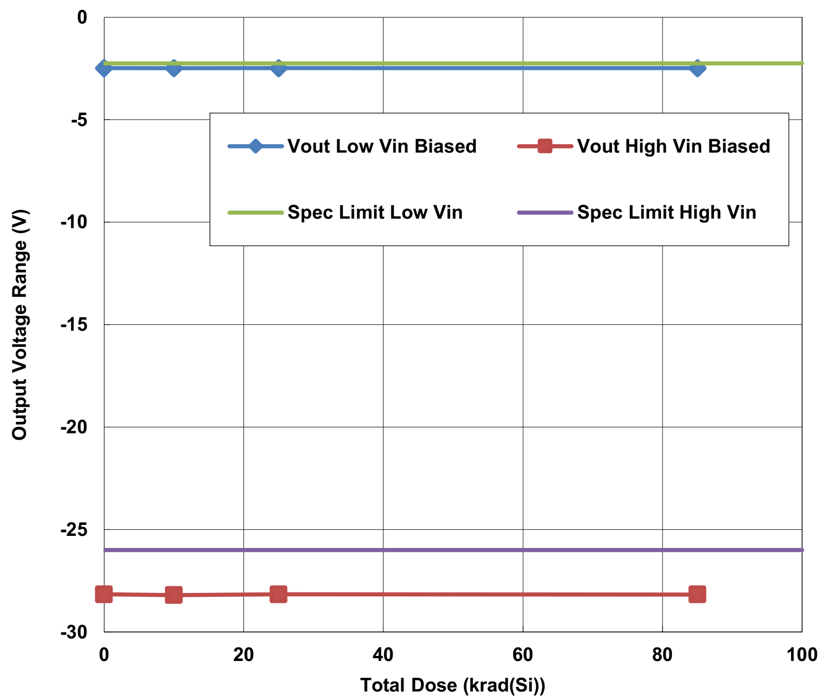


**Figure 8. ISL72991RH negative voltage regulator output voltage range at input voltages of -3V and -30V as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limits are -26V minimum (-30V case) and -2.25V minimum (-3V case).**

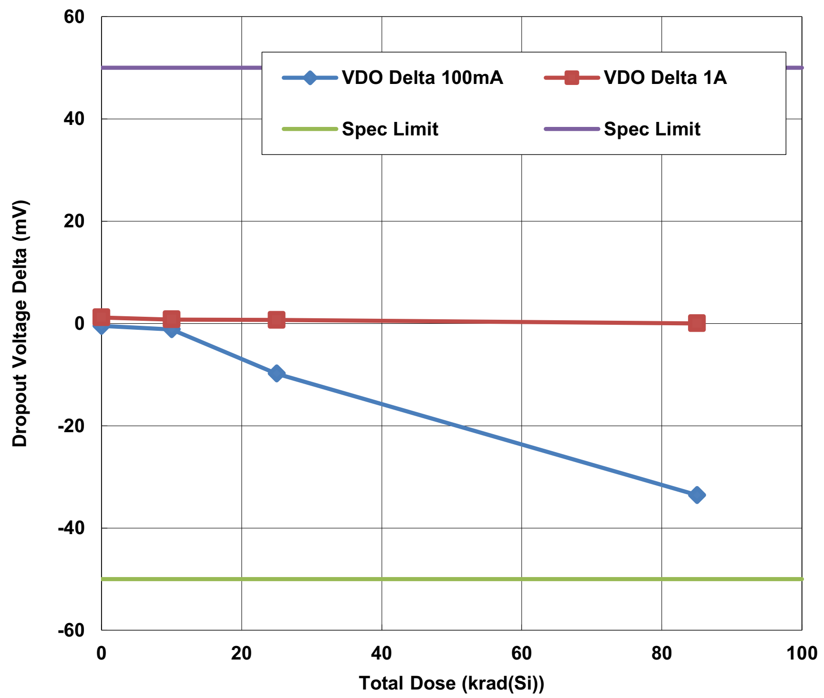


**Figure 9. ISL72991RH negative voltage regulator calculated dropout voltage measurement (dropout voltage delta') at load currents of 100mA and 1A as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. This is an ATE limit and is not specified in the datasheet or SMD; the ATE parametric limits are -50mV to 50mV. See Discussion and Conclusion for additional comments.**

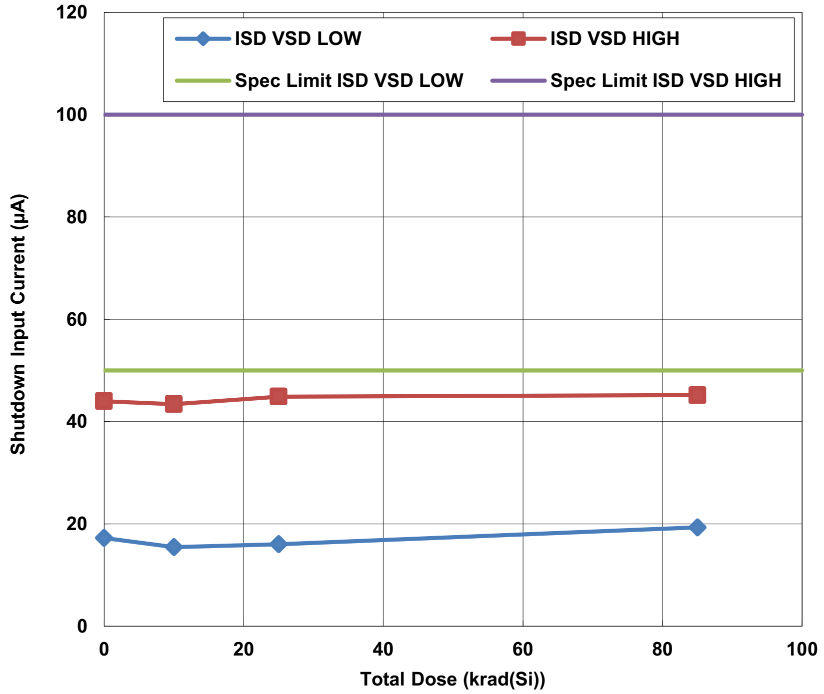


**Figure 10. ISL72991RH negative voltage regulator shutdown pin input current for the $V_{SD}$ HIGH and LOW cases, as a function of biased LDR total dose irradiation. The dose rate was 0.01rad(Si)/s and the sample size was 13. The post-radiation SMD limits are 50µA maximum ($V_{SD}$ LOW) and 100µA maximum ($V_{SD}$ HIGH).**

# 4. Discussion and Conclusion

This document reports the results of LDR TID testing of the ISL72991RH radiation hardened negative voltage regulator. This was a limited test as the part is not specified for LDR performance and an -EH version (indicating RLAT at both HDR and LDR) is not available or planned. Because of this and to capacity limitations of the R&D Shepherd 484 irradiator used at the time of testing, only a biased test was performed. The results of this test are therefore, intended as customer guidance only. Testing was completed to downpoints of 10krad(Si), 25krad(Si), and 85krad(Si). All samples showed good stability and no rejects to the SMD post-irradiation limits were encountered to the maximum TID level.

It is appropriate to comment on Figure 9, which plots an ATE-generated indirect representation of the dropout voltage at load currents of 100mA and 1A. It also gives a more accurate representation of dropout voltage stability over irradiation. The parameter showed great stability for the 1A output current case but degraded significantly for the 100mA output current case. The parameter remained well within the ±50mV ATE limits.

The ATE test sequence of the dropout voltage measurement is as follows:

1. With an input voltage of -7.0V, the regulator output voltage is set to -5.0V by connecting a 1.2K resistor from the SET pin to ground. The output load current is set to 100mA and the output voltage is measured, with an expected value close to -5V. The output voltage is labeled $V_{OUT1}$ and stored. With a drop across the pass transistor of about 2V, the pass transistor is well out of saturation in this configuration and the regulator is not in a low dropout voltage state.
2. Next, the regulator input voltage is set using Equation 1, which uses the stored $V_{OUT1}$ value.

**(EQ. 1)** $$V_{IN} = V_{OUT1} - 200mV$$

   In this configuration, the regulator output is still set at -5V, but the input voltage is reduced to within 200mV of that output voltage. This places the regulator in the LDO mode; the pass transistor saturates, and the drop across the pass transistor approaches the offset voltage of the transistor. The 200mV represents the maximum post-radiation dropout voltage specification for 100mA load current.
3. Next, the regulator output voltage is measured again. It should be within 50mV of the value of $V_{OUT1}$ as measured in Step 1. Differences in excess of 50mV indicate that the dropout voltage is in excess of 200mV and that the regulator is starting to drop out of regulation.
4. This procedure is repeated for a load current of 1A and a maximum dropout voltage value of 1V. Again, the maximum output voltage change is 50mV.

# 5. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | Jun 23, 2021 | Initial release |

# Appendix: Reported Parameters and Figures

**Table 2. Key Total Dose Parameters**

| Fig. | Parameter | SMD Symbol | Low Limit | High Limit, | Units |
|---|---|---|---|---|---|
| 2 | Reference voltage | VREF | -1.279 | -1.231 | V |
| 3 | Quiescent power supply current | IQDO | -5 | 25 | mA |
| 4 | Adjust pin current | IADJ | - | 5 | µA |
| 5 | Line regulation | VLNR | -25 | 25 | mV |
| 6 | Load regulation | VLDR | -12 | 12 | mV |
| 7 | Output current limit | ICL | 600 | 900 | mA |
| 8 | Output voltage range | VO (-3V in) | -2.25 | - | V |
| | Output voltage range | VO (-30V in) | -26 | - | V |
| 9 | Dropout voltage delta (ATE parameter) | VDO_DEL_100mA | -50 | 50 | mV |
| | Dropout voltage delta (ATE parameter) | VDO_DEL_1A | -50 | 50 | mV |
| 10 | Shutdown pin input current | ISD (VSD LOW) | - | 50 | µA |
| | Shutdown pin input current | ISD (VSD HIGH | - | 100 | µA |

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