Release Note

SSP v2.6.0

Release Note

Renesas Synergy™ Platform
Synergy Software
Synergy Software Package

Renesas Electronics
www.renesas.com

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Renesas Synergy™ Platform

SSP v2.6.0 Release Note

Contents

1. Introduction

This document describes the release notes for **Synergy Software Package (SSP) version 2.6.0**.

2. Release Information

SSP Release Version	v2.6.0
Release Date	Mar 29, 2024

The intended audience for this release note is Renesas Synergy™ customers, prospective customers, partners, and support staff. This release note describes the enhancements, fixed issues and known issues in SSP v2.6.0.

Note: All SSP v2.0.0 and later releases no longer require a Synergy license key.

3. Synergy MCU Groups Supported

MCU Groups: S7G2, S5D9, S5D5, S5D3, S3A7, S3A6, S3A3, S3A1, S128, S124, and S1JA.

4. Software Tools and Hardware Kits Supported with this SSP Release

Tool	Version	Description	Remarks
e² studio	2024-01.1	Software development and debugging tool.	e² studio for Synergy standalone installer is no longer provided on the website. If needed, please use Renesas Knowledge Base and enter a ticket request.
IAR Embedded Workbench® for Renesas Synergy™	8.23.3	Software development environment and debugging tool.	Renesas no longer distributes IAR tool chain, contact IAR: https://www.iar.com/products/architectures/renesas/iar-embedded-workbench-for-renesas-synergy/
SSC	2024-01.1	Synergy Standalone Configurator. Used in combination with IAR EW for Synergy.	Available here for downloading: https://www.renesas.com/in/en/software-tool/renesas-synergy-standalone-configurator-ssc
GNU Arm Compiler	GCC 10.3-2021.10	GNU compiler is an open-source compiler provided by Arm®	https://developer.arm.com/tools-and-software/open-source-software/developer-tools/gnu-toolchain/gnu-rm/downloads
IAR Compiler	8.23.3	IAR Arm® compiler toolchain	Renesas no longer distributes IAR tool chain, contact IAR: https://www.iar.com/products/architectures/renesas/iar-embedded-workbench-for-renesas-synergy/
QE for Capacitive Touch	v3.3	Development Assistance Tool for Capacitive Touch Sensors	https://www.renesas.com/us/en/software-tool/qe-capacitive-touch-development-assistance-tool-capacitive-touch-sensors
RYZ014A Pmod	v01	Expansion board for RYZ014A module	RTKYZ014A0B00000BE - PMOD Expansion Board for RYZ014A | Renesas

Tool	Version	Description	Remarks
PE-HMI1	2.0	Product Example (PE) for Human Machine Interface to evaluate Renesas Synergy™ S7G2 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/yspehmi1s20ws2j-pe-hmi1-product-example
DK-S7G2	4.1	Development Kit for Renesas Synergy™ S7G2 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ysdks7g2e40-dk-s7g2-development-kit
SK-S7G2	3.3	Starter Kit for Renesas Synergy™ S7G2 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/yssks7g2e30-sk-s7g2-starter-kit
PK-S5D9	1.0	Promotion Kit for Renesas Synergy™ S5D9 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/yspks5d9e10-pk-s5d9-promotion-kit
TB-S5D5	1.2	Target Board Kit for Renesas Synergy™ S5D5 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ystbs5d5e10-tb-s5d5-target-board-kit
TB-S5D3	1.2	Target Board Kit for Renesas Synergy™ S5D3 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ystbs5d3e10-tb-s5d3-target-board-kit
DK-S3A7 (Obsolete – do not use for new designs)	2.0	Development Kit for Renesas Synergy™ S3A7 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ysdks3a7e20-dk-s3a7-development-kit
TB-S3A6	1.2	Target Board Kit for Renesas Synergy™ S3A6 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ystbs3a6e10-tb-s3a6-target-board-kit

Tool	Version	Description	Remarks
TB-S3A3	1.2	Target Board Kit for Renesas Synergy™ S3A3 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ystbs3a3e10-tb-s3a3-target-board-kit
TB-S3A1	1.1	Target Board Kit for Renesas Synergy™ S3A1 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ystbs3a1e10-tb-s3a1-target-board-kit
DK-S128	2.0	Development Kit for Renesas Synergy™ S128 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ysdks128e10-dk-s128-development-kit
DK-S124	3.1	Development Kit for Renesas Synergy™ S124 MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ysdks124s20-dk-s124-development-kit
TB-S1JA	1.3	Target Board Kit for Renesas Synergy™ S1JA MCU Group	https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/ystbs1jae10-tb-s1ja-target-board-kit
J-Link Software	7.84d	SEGGER J-Link® debug probe is the quasi standard for Arm® Cortex®-M based MCUs	Jlink 7.84d is integrated as part of e^2 studio 2024-01.1 and SSP v2.6.0 Platform Installer.

4.1 Version Information for Third-Party Modules

Component	Version in SSP v2.6.0	Links for Azure RTOS documents and download links for GUIX Studio and TraceX
Azure RTOS ThreadX®	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/threadx/
Azure RTOS NetX™	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/netx/
Azure RTOS NetX Duo™	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/netx-duo/
Azure RTOS NetX Application bundle	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/netx/
Azure RTOS NetX Duo Application bundle	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/netx-duo/

Component	Version in SSP v2.6.0	Links for Azure RTOS documents and download links for GUIX Studio and TraceX
Azure RTOS USBX™	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/usbx/
Azure RTOS FileX®	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/filex/
Azure RTOS GUIX™	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/guix/
Azure RTOS LevelX	6.2.1	https://docs.microsoft.com/en-us/azure/rtos/levelx/
Azure RTOS TraceX[1]	6.2.1 or later	https://docs.microsoft.com/en-us/azure/rtos/tracex/ Downloadable from Microsoft App Store[1]: https://apps.microsoft.com/store/detail/azure-rtos-tracex/9NF1LFD5XXG3?hl=en-us&gl=US
Azure RTOS GUIX Studio[1]	6.2.1 or later	https://docs.microsoft.com/en-us/azure/rtos/guix/overview-guix Downloadable from Microsoft App Store[1]: https://www.microsoft.com/en-us/p/azure-rtos-guix-studio/9pbm1k1r7q0f?activetab=pivot:overviewtab
TES D/AVE 2D	3.4.0	https://www.tes-dst.com/technology-products/gpus/d/ave-2d/
CMSIS component versions	CMSIS Base v5.8.0 CMSIS Core v5.5.0 CMSIS DSP v1.9.0 CMSIS NN v3.0.0	Release CMSIS 5.8.0 ARM-software/CMSIS_5 GitHub

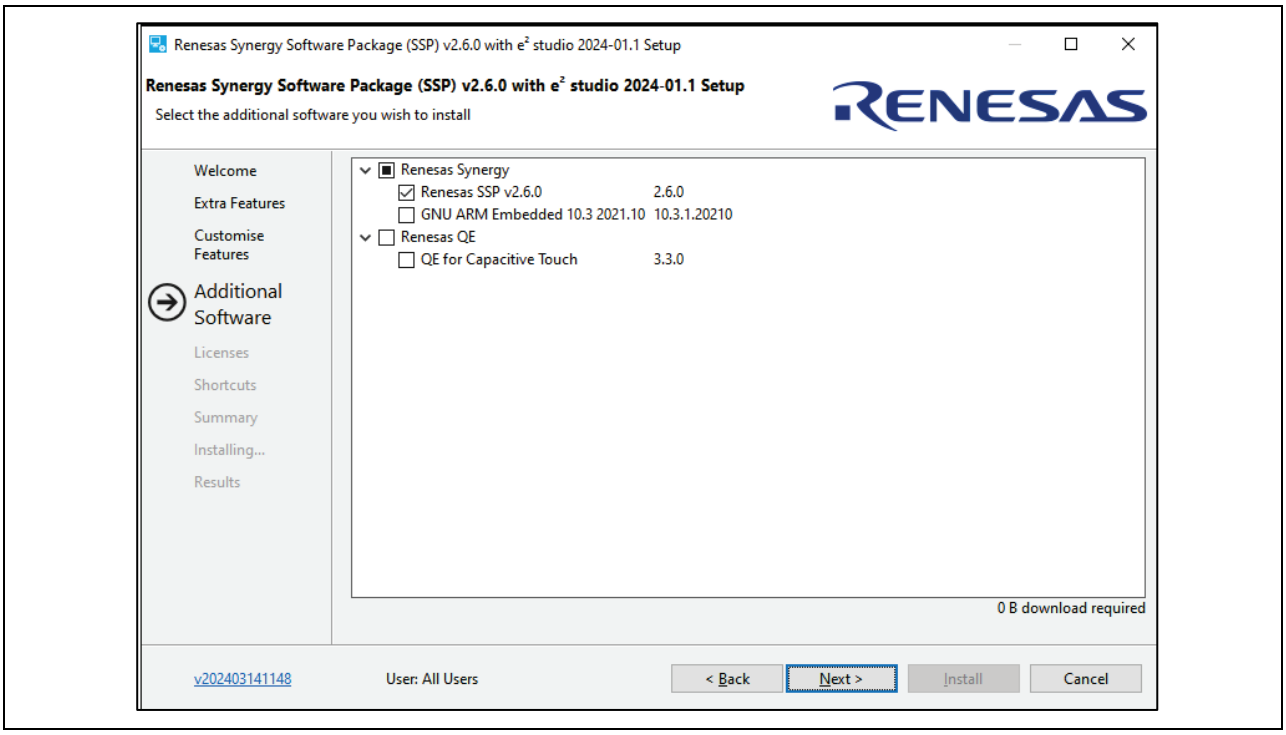
[1] Minimum system requirement is a Windows® 10 version to build 14393. Your company's IT policy may limit the installation of software from the Microsoft App Store. In such a case, contact your company's IT department.

5. SSP Release Package and Installation Information with e² studio

For installation of SSP with e² studio, please use the platform installer link provided on the SSP download page (Renesas Synergy™ Software Package (SSP)):

1. Click the Platform Installer button.
2. Select e² studio on the Select a Development Environment pop-up.
3. Read and accept the SSP Evaluation License Agreement.
4. A *.zip file will then be downloaded. Once complete, extract and run the *.exe file.
5. Choose either the Quick Install or Custom Install options:
   A. Quick Install will install **e² studio v2024-01.1, SSP v2.6.0, and GCC 10.3-2021.10** and additional components as needed.
   B. Custom Install will allow you to select the options you want to install and during the process, will allow you to deselect the GNU ARM compiler as shown in the screenshot below.

Note: The only version of the GCC compiler supported by SSP v2.6.0 is GCC 10.3-2021.10. If you must use earlier versions of the GCC compiler, please use with the recommended version of SSP and do not install SSP v2.6.0.



6. Accept the Software Agreement terms.
7. Accept the Shortcut or create your own as needed.
8. Click Install and the installation will be completed.

Important Notes:

1. The default installation folder for the SSP is C:\Renesas\Synergy.

SSP documentation is available for download from the Renesas Synergy™ Software Package (SSP) page at Renesas Synergy™ Software Package (SSP). Sign in to the MyRenesas account using your existing MyRenesas or Synergy Gallery credentials, or by creating a new MyRenesas account.

2. All SSP v2.6.0. software source code is provided without encryption, except FMI and r_sce modules which are shared as pre-built libraries.

3. e² studio does not need a License key for generating SSP v2.6.0 Projects.

6. SSP Release Package and Installation Information with SSC

Important: Only Renesas Synergy™ users who would like to use the IAR Embedded Workbench for Renesas Synergy™ as their development environment need to download and install the SSC.

To install SSC v2024-01.1, download the individual SSC v2024-01.1 installer (`.zip`) from www.renesas.com/synergy/ssc. Unzip it, then double-click the installer and follow the directions on the screen.

To use the SSC and the SSP together with IAR Embedded Workbench for Synergy, follow these steps:

1. Download SSC v2024-01.1 from www.renesas.com/synergy/ssc , unzip it, and double-click the executable file. The default installation directory is `C:\Renesas\Synergy\sc_v2024-01.1_ssp_v2.6.0`.
2. IAR Embedded Workbench for Synergy v8.23.3 is available from IAR at www.renesas.com/synergy/iar-embedded-workbench.
3. Backup the existing SSP projects before migrating to SSC v2024-01.1.

Note: With SSC platform installer both SSC and SSP 2.6.0 will be installed , user need not install SSP separately

7. Issues Fixed in SSP v2.6.0

Issue ID: 17541

There was an issue with the pin configurations tab usage in SSC v2023-07 as the configurator gave an error when changing any options in that tab.

This issue is now fixed in SSC v2024-01.1 with SSP v2.6.0.

Applies to: All MCUs

8. Known Issues and Limitations in SSP v2.6.0

8.1 BSP for SSP Supported Platforms

Issue ID: 10664

If a user is using the trace buffer for debugging and has data stored in the RAM at addresses above 0x2000 4000, that data will be overwritten by the trace buffer when debugging.

Applies to: S128 and S1JA MCU Groups

Workaround: The S128 linker script currently allocates 1K for the trace buffer at 0x2000 0000. This allocation could be removed, freeing up the 1K mistakenly reserved for the trace buffer. Using the e^2 studio trace buffer function will store 1K of the trace buffer data beginning at 0x2000 4000, so that 1K of RAM must not be used by the application if the trace buffer is to be used for debugging.

8.2 Creation of Pin Mapper Input xml Files

Issue ID: 17574

When creating a new project or changing the BSPs of an existing project, pin configurations for some peripherals may show unresolved conflicts. These conflicts do not cause any functional issue; the user can proceed to build the project.

Applies to: All MCUs

Workaround: Disable the operation mode for the peripheral and enable it again.

8.3 Crypto/r_sce

Issue ID: 15261

At times, some noticeable delay is seen during RSA 2048-bit key generation.

Applies to: S7 and S5 MCU Series

Workaround: None

8.4 FileX Development

Issue ID: 17076

When files are created in a media device using FileX and if they are operated in the Windows platform, the short file name (SFN) associated with the files will get changed. If more files are created using FileX in the same media device, FileX may end up assigning SFN which collides with the SFNs of existing files.

Applies to: S3, S5, and S7 MCU Series

Workaround: None

8.5 File System

Issue ID: 16181

If the block media is partially exFAT formatted (FileX configuration option “total_sectors” is less than the total sectors in block media, and the “File system on block media” id changed to “False”), the SD card media opens correctly in the board, file operation on the board also works correctly, but the media open fails in a PC Windows® environment.

Applies to: All MCUs

Workaround: The user has to exFAT format the complete block media to use it in a PC Windows® environment.

8.6 ISDE User Experience

Issue ID: 7665

When using the Synergy Software Configurator in e^2 studio/SSC, if you rename a thread on the Threads tab and generate code, a new `thread_entry.c` file is created with template content, and the old `thread_entry.c` file remains in the project. If you have edited the `thread_entry.c` file, your changes are not moved to the new file. The old file remains in the project. It will not be called; it causes a build error if not removed from the project manually.

Applies to: All MCUs

Workaround: Manually move any edits (if made) from the old `thread_entry.c` file to the new `thread_entry.c` file, then manually delete the old `thread_entry.c` file from your project.

Issue ID: 12826

If Synergy Configuration window is maximized in e^2 studio, the property window will not be updated.

Applies to: All MCUs

Workaround: Do not maximize the Synergy Configuration window before clicking on elements when editing the properties.

Issue ID: 12908

A multiple symbol definition error may occur during linkage if an Azure RTOS library component and the corresponding source component such as ux and ux_src are included. If this occurs, remove the library such as libux.a from the list of libraries used by the linker.

For GCC, this in the **Cross ARM C Linker** > **Libraries section of the C/C++ Build** > **Settings** in the project **Properties**.

For IAR, this in the **IAR Linker for ARM** > **Library section of the C/C++ Build** > **Settings** in the project **Properties**.

Module Names: ux (USBX), tx (ThreadX), nx (NetX), nxd (NetX Duo), fx (FileX), gx (GUIX), ux_host_class_XXX (USBX Host Classes), ux_device_class_XXX (USBX Device Classes).

Applies to: All supported MCU Groups

Issue ID: 13854

When debugging a project with a large number of threads (for example, 150 threads) with the RTOS Resource View open, e^2 studio might hang and become unresponsive.

Applies to: All MCUs

Workaround: Make the RTOS Resource View small and expand it once the Debug Tree View has finished updating.

8.7 NetX and NetX Duo

Issue ID: 7745

The NetX/NetX Duo FTP Client requires FileX in stack configuration. Due to dependencies, FileX cannot be removed from the configurator while using FTP_Client application.

Applies to: S7G2, S5D9, and S5D5 MCU Groups

Workaround: None

Issue ID: 14293

Build warnings will be observed on compiling NetX Duo BSD application with GCC v7.x compiler.

Applies to: CM4 MCUs (S7, S5, and S3 MCU Series)

Workaround: None

Issue ID: 16888

New features introduced in SSP released are enabled by default. This may cause existing applications to exceed the maximum available memory space of the selected MCU causing memory overflow errors.

Applies to: All MCUs

Workaround: Use the configurator to disable any unused options and rebuild the application. For example, in SSP v2.1.0, support for ECC P-224 and P-384 ciphers is added and these are enabled by default. If an application using r_sce that built successfully prior to SSP v2.1.0 now fails to build with SSP v2.1.0 due to memory overflow, this may be due to the newly added ECC cipher support. This can be fixed by choosing the SCE Common driver on r_sce in the e^2 studio Threads Configuration view and disabling all cipher types and key lengths that are not used by the application.

8.8 r_agt_input_capture

Issue ID: 15070

While capturing pulse width with AGT input capture, after a measurement completion, the counter and overflow value returned from callback are fine, but the same values read simultaneously with `lastCaptureGet` API are incorrect.

Applies to: All MCUs

Workaround: None

8.9 r_rspi

Issue ID: 16700

The RSPI SPI module uses the DTC as the low level transfer driver. If the DMAC and the DTC are contending for the DMA bus the DMAC always uses a high priority. Thus a DTC based SPI transfer from RSPI module will not get access to the DMA bus since the DMAC is already using it. This will cause the SPI to go into the IDLE mode and trigger a TEND interrupt event. Since at this point the TEND interrupt is disabled, the interrupt remains in the pending state. When the DTC transfer finishes, the CPU will receive the TX interrupt to finish the transfer and then will enable the TEND interrupt. The pending TEND interrupt causes the SPU transfer to be ended early.

Applies to: All MCUs

Workaround: This is a limitation of the RSPI module and the issue can be avoided by not using the DMAC while the DTC is being used by the RSPI module.

8.10 r_sci_spi

Issue ID: 15574

In an application, if using DTC for data transfer, SCI SPI can experience overrun error if the same application makes heavy use of DMAC and/or another DTC instance. This is because DMAC has a high priority over DTC in arbitration for the mastership of the DMA bus. Also, arbitration between different triggers/transfers in DTC is done based on interrupt/trigger priority. So, if the DMAC or DTC triggered by high priority interrupt/task is accessing the DMA bus and SCI SPI receiving the data at the same time, DTC used by SCI SPI will not be able to access the bus to transfer the received data into the memory, causing SCI SPI to return overrun error.

Applies to: All MCUs

Workaround: Overrun error can be averted with one of the following options:

1. If SCI SPI uses DTC for data transfer, avoid the use of DMAC or another DTC instance in an application.
2. If DMAC/DTC is a must for other data transfers, avoid the use of DTC with SCI SPI.
3. Use the RSPI instead of SCI SPI. The RSPI hardware can handle overrun conditions.

8.11 sf_ble

Issue ID: 9225

HID profile client mode is not supported by RL78G1D. As a result, the BLE framework implementation of the HID profile will also not support the HID profile client mode. Applications using a BLE framework for RL78G1D will not be able to use the HID profile in client mode.

Applies to: All MCUs

Workaround: None

Issue ID: 9256

The projects using RL78G1D framework will see compilation warnings. All the warnings are in the RL78G1D driver code and will not have impact on the user applications. The RL78G1D framework files do not have any warnings.

Applies to: RL78G1D on all Synergy MCUs

Workaround: None

8.12 sf_cellular

Issue ID: 14565

PAP/CHAP authentication fails on the network where authentication is enabled. PAP callback is not working when PAP authentication is enabled in the configurator.

Applies to: S7, S5, S3 MCU Series

Workaround: None

Issue ID: 14566

Automatic time zone update disable functionality does not work. Even when the user disables automatic time zone update, the current updated time is received.

Applies to: Quectel BG96 modules

Workaround: None

8.13 sf_el_fx records

Issue ID: 17016

When creating more than 26 files using `fx_file_unicode_create()` API, the service returns FX_ALREADY_CREATED error code from the 27th time.

Applies to: S3, S5, and S7 MCU Series

Workaround: None

8.14 sf_el_gx

Issue ID: 15783

Build warnings are being observed when compiling GUIX Source with GCC 7.2.1.

Applies to: S7G2 and S5D9 MCU Groups

Workaround: None

8.15 sf_el_nx

Issue ID :7513

Current sf_el_nx NetX Port driver is hard-coded to use RMMI interface which is for a Micrel Ethernet PHY chip mounted on Renesas kits but does not support the other PHY chips or MMI interface. Customer need to define their own Ethernet PHY chip driver if they use a different PHY chip from the one mounted on Renesas kits, or use a PHY chip with MII interface.

Applies to: All MCUs

Workaround:

Currently there is no plan to provide support for other Ethernet PHY chip drivers in SSP, users should create their custom PHY chip driver using the reference driver provided in SSP. To do that, you can utilize sf_el_nx (NetX Port) module under `/ssp/src/framework/sf_el_nx/` as a template and modify it for your Ethernet PHY chip. Also include an interface file `sf_el_nx.h` located at `/ssp/inc/framework/instances/` in the created new PHY chip driver. Source files under sf_el_nx are plain text so you can copy the file to other directories, such as /src/ directory and exclude original sf_el_nx module from building to avoid 'multiple definition' compile-error.

Here is the brief guideline to work around the issue:

- Copy the directory `/ssp/src/framework/sf_el_nx/` including all the files under the directory to /src/.
- Exclude original SF_EL_NX module in SSP from your build. Right click on the directory `/ssp/src/framework/sf_el_nx/` and select '**Exclude from build…**'. Then click '**Select All**' button.
- Modify `/src/sf_el_nx/nx_hw_init.c`. `nx_synergy_ethernet_init()` needs modification below to select MII interface. Change IOPORT_ETHERNET_MODE_RMII to IOPORT_ETHERNET_MODE_MII.g_ioport_on_ioport.pinEthernetModeCfg(IOPORT_ETHERNET_CHANNEL_n, IOPORT_ETHERNET_MODE_RMII);
- Modify `/src/sf_el_nx/phy/ether_phy.c` and `ether_phy.h`. These files need modification to match to your Ethernet PHY chip.
- Make sure selecting MII pins under **Pins** tab in Synergy Configurator. Check pin configuration setting; **Peripherals** > **Connectivity:ETHERC**.

Notes:

- Source files under `/ssp/src/framework/sf_el_nx/` will be overwritten by tool when building a project so you should copy the files before - Source files under `/ssp/src/framework/sf_el_nx/` will be overwritten by tool when building a project so you should copy the files before your editing.
- To exclude files from building, right-click on the files and select '**Exclude from build..**' (this is the case for e^2 studio).

Module Name: SF_EL_NX (NetX Port)

8.16 sf_el_tx

Issue ID: 13678

SF_CONTEXT_SAVE and SF_CONTEXT_RESTORE (in `bsp_common.h`) should only be defined if TX_ENABLE_EXECUTION_CHANGE_NOTIFY or TX_ENABLE_EVENT_TRACE is defined.

Applies to: All MCUs

Workaround: None

8.17 sf_el_ux

Issue ID: 8574

The current sf_el_ux HCD driver does not enable the double buffer feature for bulk out PIPEs, which is supported by USB hardware. Because of that, USB data throughput for data write through a bulk out PIPE will be less than the value for double buffer-enabled. This issue is only for data write (bulk OUT). Double buffering is supported for data read (bulk IN).

Applies to: S7, S5, and S3 MCU Series

Workaround: None

Issue ID: 13481

The USB host sends out a PING packet after receiving NAK or NYET handshake from the device. However, it also sends out a PING packet for ACK handshake, which is not expected behavior according to the USB 2.0 specification.

Applies to: All MCUs supporting USBX Host

Workaround: None

Issue ID: 16572

In `sf_el_ux` device class driver, there is a redundant semaphore for 'device transfer request' that needs to be removed. Common semaphore can be used for the device transfer request for both S1 MCU Series and S3, S5, S7 MCU Series instead of using two semaphores - one for S1 MCU series and another for S3, S5 and S7 MCU Series separately.

Applies to: All MCUs

Workaround: None

8.18 sf_Wifi

Issue ID: 8394

The projects using GT202 framework will see compilation warnings. All the warnings are in the 3rd party GT202 driver code. The GT202 framework files do not have any warnings. The warnings should not impact the user applications.

Applies to: WiFi Framework for GT202 on S7G2, S3A7, S5D9, S5D5, S3A6 (only socket), S3A3 MCU Groups

Workaround: None

Issue ID: 12742

GT202 module supported by WiFi Framework is affected by WPA2 KRACK issue.

Applies to: GT202 module supported by WiFi Framework

Workaround: None

Issue ID: 14126

WiFi WPS functionality does not work with WPA security.

Applies to: WiFi Framework using GT202

Workaround: None

8.19 sf_wifi_qca4010

Issue ID: 16558

SF_WIFI_QCA4010 framework does not support WPS method of provisioning.

Applies to: S3, S5, S7 MCU Series

Workaround: None

8.20 SSP IAR Support

Issue ID: 13900

In some cases, the build fails with the error “Secure builder required” after migrating to a newer SSP version in EWSYN.

Applies to: All MCUs

Workaround: Select **Project** > **Make** (F7) after the issue occurs. The project should then build without errors.

Issue ID: 14485

Library projects which use many/long `include` paths cause the compiler command line to exceed system limit and fails to build the library.

Applies to: Projects created with IAR compiler in e^2 studio.

Workaround: None

Issue ID: 16723

If using the IAR compiler from IAR EWSYN product, but invoked from e^2 studio IDE, installing the IAR Embedded Workbench plugins into e^2 studio may result in the following message:

“Warning: Installing unsigned software for which the authenticity or validity cannot be established. Continue with installation?”

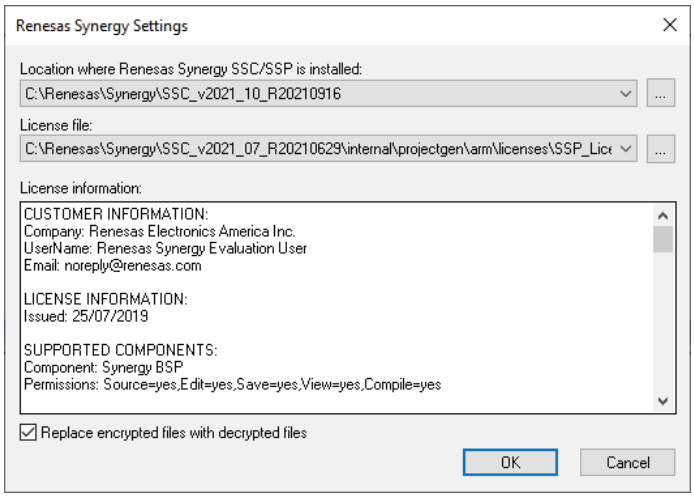
Applies to: All MCUs

Workaround: This warning can be ignored – click on the “Install anyway” option to continue with the installation.

Issue ID: 16988

Synergy License file information is no longer required for SSP v2.x. The Renesas Synergy™ settings dialog in IAR Embedded Workbench for Synergy shows the License information section to support any imported SSP v1.x projects.

SSP Evaluation License is located in the following directory:
`<SSC_base_dir>\internal\projectgen\arm\Licenses\.`



Applies to: All MCUs

Workaround: None

8.21 SSP XMLs for ISDEs

Issue ID: 10695

Configurator does not warn about the limitation on RSPI bit rate if it is less than or equal to 30 MHz.

Applies to: All MCUs

Workaround: RSPI bit rate must be a positive integer less than or equal to 30 MHz or PCLK/2, whichever is minimum.

Issue ID: 12857

Creating a project with a custom board pack might not reflect the customized values set for the properties in that custom board pack.

Applies to: All MCUs

Workaround: None

8.22 TES

Issue ID: 14095

The rendering of concave polygons is not supported when D/AVE 2D drawing engine is enabled.

Applies to: S7G2 and S5D9 MCU Groups

Workaround: Disable D/AVE 2D drawing engine to render concave polygons.

Issue ID: 15762

An application using pixelmaps to fill the shapes does not render pixelmaps properly inside the shapes if the pixelmaps width and height are not the power of 2.

Applies to: S7G2 and S5D9 MCU Groups

Workaround: The pixelmaps are properly drawn inside the shapes if pixelmap width and height are the power of 2.

8.23 USBX

Issue ID: 8647

The USB throughput for file `read/write` operation with USBX Device Class Mass Storage is not consistent and may vary for every measurement.

Applies to: All MCUs

Workaround: None

Issue ID: 17096
The `sf_el_ux_comms_v2 Write` API sends a ZLP packet after it sends the requested bytes, for all requested lengths, instead of sending ZLP only when the requested length is a Multiple of `wMaxPacketSize`. There is no functionality impact because of this, but this is an undesired behavior.

Applies to: All MCUs

Workaround: None

8.24 Known Issues in Synergy Development Tools

8.24.1 Pin Mapping Issues

Issue ID: 12261

DAC8 output pin is not configured when it is configured through ISDE as the pin configuration does not support setting ASEL and PSEL bit fields for the same pin.

Applies to: S1JA, S128, and S3A3 MCU Groups

Workaround: Configure DAC8 output pin manually.

Update `g_ioport_on_ioport.pinCfg` setting on the pin configured for DAC by adding the following:

```
| IOPORT_CFG_PERIPHERAL_PIN | IOPORT_PERIPHERAL_CAC_AD
```

Issue ID: 14088

When setting the IRQ on the GPIO pin, there is no conflict shown if the IRQ is already assigned to another pin.

Applies to: All MCUs

Workaround: Manually check the ICU peripheral to see if the IRQ is already assigned to a pin before setting it to a GPIO pin.

Issue ID: 16561

The VREFH pin for the S1JA device cannot be configured but the VREFL pin is configurable without errors through the pin configurator. When generating the project content, `pin_data.c` file does not have the data for the pin configured. The user needs to manually add the data.

Applies to: S1JA MCU Group, and S3 MCU Series

Workaround: The user will have to manually configure the VREF pins for S1JA MCUs through the IO port API in their application, for example, `g_ioport.p_api -> pincfg(OPPORT_PORT_00_PIN_10, IOPORT_CFG_ANALOG_ENABLE);`

Issue ID: 16592

Migrating a SSP v1.x project that has the comparator functions configured, to SSP v2.x does not work properly.

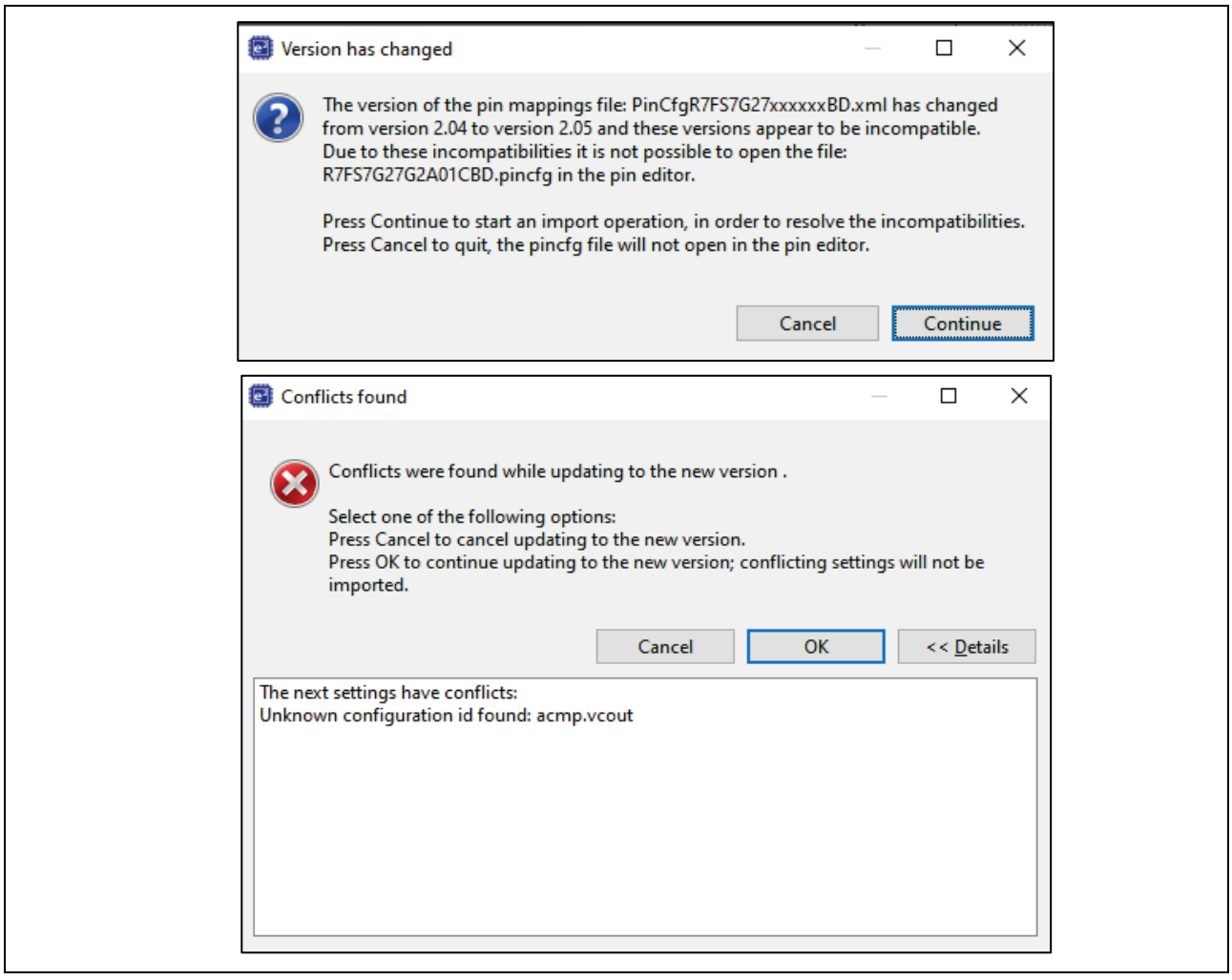
One of the following issues will be noticed:

1. Pin editor does not open and complains about the invalid `pinmapping.xml` file.
2. Shows messages about conflicts found.
3. Migrates with error in pin configuration.

Applies to: All MCUs

Workarounds (corresponding to items 1,2, and 3 in the issue description above, respectively):

1. **Option 1**: Manually recreate the configuration in SSP v2.x.
   Option 2: Remove the configuration for CMP function and then migrate to SSP v2.x.
2. Click **Continue** and **OK** on the messages shown below to continue to migrate the project. The project migrates with an error. Manually fix the error in the ACMP function (for example, by selecting the pin for VCOUT on ACMP0).
3. Manually fix the error in the ACMP function (for example, setting the operation mode).



4. Manually fix the error in the ACMP function (for example, by setting the operation mode).

8.24.2 Synergy Tools

Issue ID: 11556

Synergy builder is excluded from the tool command pattern when changing the toolchain from IAR 7.x to IAR 8.x, which leads to a build error that the secure builder is required when trying to build the project after migrating.

Applies to: All MCUs

Workaround:

The following workaround can be used to migrate projects with IAR 7.x to IAR 8.x:

1. Add environment variable `SECURE_BUILD_COMMAND`: `${renesas.support.targetLoc:synergy-build} /isdebuild`
2. Update command line pattern IAR C/C++ Compiler for ARM setting if the following command is missing: `${SECURE_BUILD_COMMAND}`
3. Update command line pattern IAR C/C++ Assembler for ARM if the following command is missing: `${SECURE_BUILD_COMMAND}`

Issue ID: 12584

An error occurs when setting the watchpoint at certain addresses. Debug sessions cannot be started when these watchpoints with errors are still present.

Applies to: S5D9 MCU Group

Workaround: Remove the watchpoints from the breakpoints view and start the debug session.

Issue ID: 12925

When exporting the project, selecting the option for .tar format does not export the project in `.tar` format, but exports it in `.zip` format.

Applies to: Tools

Workaround: Edit the archive file name field by replacing the `.zip` with `.tar`, and the project will be exported in `.tar` format.

Issue ID: 14436

Some of the old projects with customized stacks might fail after migrating to e^2 studio v7.3 or later versions because the default modules get repopulated in the stack.

Applies to: All MCUs

Workaround: The user explicitly needs to delete the modules that are repopulated after migration.

Issue ID: 15339

Default property value of the IP address does not get picked up for existing projects after changes to the pack. Opening existing projects shows the previously saved value instead of the default value from the pack.

Applies to: Projects which use the packs with the change for IP address

Workaround: None

Issue ID: 17055

Developer Assistance for API reference for r_ctsuv2 module is not available.

Applies to: All MCUs

Workaround: None

Issue ID: 17237

SSC does not provide a Save button to save changes to the Synergy project configuration.

Applies to: All MCUs

Workaround: Click **Ctrl-S** to save the Synergy Configuration or close the SSC and click **Yes** in the Save Resource dialog to save your changes.

9. Complete List of Modules Supported in this Release

These modules are available on the respective MCUs based on the following criteria:

- If the core functionality of the module has been tested and works on an MCU, even if it has known issues, then the module is supported on the MCU.
- If the core functionality is broken or not tested on an MCU, then that module is not supported on the MCU.
- If a module is independent of the underlying MCU hardware or HAL drivers, and has been tested on a particular Synergy MCU, the following table indicates that this module is supported on all the Synergy MCUs that the underlying driver/framework/stack depend on have been tested.

9.1 BSP and Driver Modules Available in this Release

Module Name	SSP Feature	Supported Synergy MCU Groups
BSP	Board Support Package	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_acmphs	Analog Comparator High Speed	S1JA, S3A7, S5D9, S5D5, S5D3, S7G2
r_acmplp	Analog Comparator Low Power	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_adc	A/D Converter	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_agt	Asynchronous General Purpose Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_agt_input_capture	AGT Input Capture	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_analog_connect	Analog Connect	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cac	Clock Frequency Accuracy Measurement Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_can	Controller Area Network	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_cgc	Clock Generation Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_crc	Cyclic Redundancy Check Calculator	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_ctsuv2	Capacitive Touch Sensing Unit Version 2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dac	Digital to Analog Converter	S124, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dac8	8-bit Digital to Analog Converter	S128, S1JA, S3A1, S3A3, S3A6
r_dmac	Direct Memory Access Controller	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_doc	Data Operation Circuit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_dtc	Data Transfer Controller	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_elc	Event Link Controller	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_flash_hp	Flash Memory, High Performance	S5D3, S5D5, S5D9, S7G2
r_flash_lp	Flash Memory, Low Power	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_fmi	Factory Microcontroller Information	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_glcd	Graphics LCD Controller	S5D9, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
r_gpt	General Purpose Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_gpt_input_capture	General Input Capture	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_icu	Interrupt Controller Unit	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_ioport	General Purpose I/O Ports	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_iwdt	Independent Watchdog Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_jpeg_common	JPEG Common	S5D9, S7G2
r_jpeg_decode	JPEG Decode	S5D9, S7G2
r_jpeg_encode	JPEG Encode	S5D9, S7G2
r_kint	Keyboard Interrupt Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_lpmv2_s1ja	Low Power Mode V2 for S1JA	S1JA
r_lpmv2_s124	Low Power Mode V2 for S124	S124
r_lpmv2_s128	Low Power Mode V2 for S128	S128
r_lpmv2_s3a1	Low Power Mode V2 for S3A1	S3A1
r_lpmv2_s3a3	Low Power Mode V2 for S3A3	S3A3
r_lpmv2_s3a6	Low Power Mode V2 for S3A6	S3A6
r_lpmv2_s3a7	Low Power Mode V2 for S3A7	S3A7
r_lpmv2_s5d3	Low Power Mode V2 for S5D3	S5D3
r_lpmv2_s5d5	Low Power Mode V2 for S5D5	S5D5
r_lpmv2_s5d9	Low Power Mode V2 for S5D9	S5D9
r_lpmv2_s7g2	Low Power Mode V2 for S7G2	S7G2
r_lvd	Low Voltage Detection Driver	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_opamp	Operational Amplifier	S128, S1JA, S3A1, S3A3, S3A6, S3A7
r_pdc	Parallel Data Capture Unit	S5D5, S7G2
r_ptp	Precision Time Protocol	S5D9, S7G2
r_qspi	Quad Serial Peripheral Interface	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
r_riic	IIC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_riic_slave	IIC Slave	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_rspi	Serial Peripheral Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_rtc	Real-time Clock	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_i2c	Serial Communication Interface I2C	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_spi	Serial Communication Interface SPI	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sci_uart	Serial Communication Interface UART	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sdadc	Sigma Delta ADC	S1JA
r_sdmmc	SDHI Driver for SDIO and SD/MMC Memory Devices	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
r_slcdc	Segment LCD Controller	S3A1, S3A3, S3A6, S3A7

Module Name	SSP Feature	Supported Synergy MCU Groups
r_ssi	(Inter-IC Sound) Interface [old: Serial Sound Interface] or r_i2s	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_wdt	Watchdog Timer	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
r_sce[1]	Cryptographic Library (HAL interfaces)	See table note on Cryptographic Functions

[1]Cryptographic Functions: Section 9.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r_sce/cryptographic library.

9.2 Framework Modules Supported in this Release

Module Name	SSP Feature	Supported Synergy MCU Groups
sf_adc_periodic	Periodic Sampling ADC	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback	Audio Playback	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback_hw_dac	Audio Playback HW DAC	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_playback_hw_i2s	Audio Playback HW I2S	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_record_adc	Audio Record ADC	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_audio_record_i2s	Audio Record I2S	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_ble_rl78g1d	BLE Framework	S124, S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_ble_rl78g1d_onboard_profile	BLE Framework Onboard Profiles	S124, S128, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_lx_nor	Block Media Interface for LevelX NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_qspi	Block Media Interface for QSPI	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_ram	Block Media Interface for RAM	S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_block_media_sdmmc	Block Media Interface for SD Multi Media Card	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_comms_telnet	Telnet Communications	S5D3, S5D5, S5D9, S7G2
sf_console	Console	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_fx	Synergy FileX interface	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_gx	Synergy GUIX Interface	S5D9, S7G2
sf_el_lx_nor	Synergy LevelX NOR Interface	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_nx	Synergy NetX Interface	S5D5, S5D9, S7G2
sf_el_ux	Synergy USBX Interface	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_ux_comms_v2	Synergy USBX Communication Interface V2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_external_irq	External Interrupt	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
sf_i2c	I2C Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_jpeg_decode	JPEG Decode	S5D9, S7G2
sf_memory_qspi_nor	Memory QSPI NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
sf_message	Inter-Thread Messaging	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_power_profiles_v2	Power Mode Profile V2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_spi	SPI Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_tes_2d_drw	2D Drawing Engine Framework	S5D9, S7G2
sf_thread_monitor	Thread Monitor (Watchdog)	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_touch_ctsuv2	Capacitive Touch Sensing Unit Version 2	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_touch_panel_v2	Touch Panel Version 2	S5D9, S7G2
sf_uart_comms	UART Framework	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_wifi_gt202	Wi-Fi Framework	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_wifi_gt202_onchip	Wi-Fi Framework on Chip Stack	S124, S128, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_cellular_catm1	Cellular Framework Quectel BG96 CATM1	S5D9, S7G2
sf_cellular_catm1_socket	Cellular Framework Quectel BG96 CATM1 Socket	S5D9, S7G2
sf_cellular_ryz014catm1	Cellular Framework RYZ014 CAT M1	S7G2
sf_cellular_ryz014catm1_socket	Cellular Framework RYZ014 CAT M1 Socket	S7G2
sf_crypto[2], [3]	Cryptographic Framework	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
sf_el_nx_crypto	Cryptographic Framework-Shim layer	S5D3, S5D5, S5D9, S7G2
sf_wifi_qca4010	Wi-Fi QCA4010 Framework	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

[2] Cryptographic Functions: Section 9.4 lists cryptographic functions available for each MCU in this release; these functions are accessible as part of r_sce/cryptographic library.

[3] Framework Interfaces for Cryptographic Functions (sf_crypto) available for this release include: HASH, TRNG, and Key Generation (RSA and AES).

9.3 Third-Party Modules Supported in this Release

Module Name	SSP Feature	Supported Synergy MCU Groups
fx	Azure RTOS FileX	S124, S3A3, S3A6, S3A7, S5D9, S7G2
gx	Azure RTOS GUIX	S5D9, S7G2
nx	Azure RTOS NetX	S5D9, S7G2

Module Name	SSP Feature	Supported Synergy MCU Groups
nx_auto_ip	Azure RTOS NetX Auto IP	S5D9[2], S7G2
nx_bsd	Azure RTOS NetX BSD	S5D9[2], S7G2
nx_dhcp_client	Azure RTOS NetX DHCP Client	S5D9[2], S7G2
nx_dhcp_server	Azure RTOS NetX DHCP Server	S5D9[2]
nx_dns_client	Azure RTOS NetX DNS Client	S5D9[2], S7G2
nx_ftp_client	Azure RTOS NetX FTP Client	S5D9[2], S7G2
nx_ftp_server	Azure RTOS NetX FTP Server	S5D9[2], S7G2
nx_http_client	Azure RTOS NetX HTTP Client	S5D9[2], S7G2
nx_http_server	Azure RTOS NetX HTTP Server	S5D9[2], S7G2
nx_pop3	Azure RTOS NetX POP3	S5D9[2], S7G2
nx_ppp	Azure RTOS NetX PPP	S5D9[2], S7G2[2]
nx_smtp_client	Azure RTOS NetX SMTP Client	S5D9[2], S7G2
nx_snmp	Azure RTOS NetX SNMP	S5D3[2], S5D5[2], S5D9[2], S7G2
nx_sntp_client	Azure RTOS NetX SNTP Client	S5D9[2], S7G2
nx_telnet_client	Azure RTOS NetX Telnet Client	S5D9[2], S7G2
nx_telnet_server	Azure RTOS NetX Telnet Server	S5D9[2], S7G2
nx_tftp_client	Azure RTOS NetX TFTP Client	S5D9[2], S7G2
nx_tftp_server	Azure RTOS NetX TFTP Server	S5D9[2], S7G2
nxd	Azure RTOS NetX Duo Stack	S5D9, S7G2
nxd_auto_ip	Azure RTOS NetX Duo Auto IP	S5D9[2], S7G2
nxd_bsd	Azure RTOS NetX Duo BSD	S5D9[2], S7G2
nxd_dhcp	Azure RTOS NetX Duo DHCP IPv4 Client	S5D9[2], S7G2
nxd_dhcp	Azure RTOS NetX Duo DHCP IPv6 Client	S5D9[2], S7G2
nxd_dhcp_server	Azure RTOS NetX Duo DHCP IPv4 Server	S5D9[2], S7G2
nxd_dhcp_server	Azure RTOS NetX Duo DHCP IPv6 Server	S5D9[2], S7G2
nxd_dns	Azure RTOS NetX Duo DNS Client	S5D9[2], S7G2
nxd_ftp_client	Azure RTOS NetX Duo FTP Client	S5D9[2], S7G2
nxd_ftp_server	Azure RTOS NetX Duo FTP Server	S5D9[2], S7G2
nxd_http_client	Azure RTOS NetX Duo HTTP Client	S5D9[2], S7G2
nxd_http_server	Azure RTOS NetX Duo HTTP Server	S5D9[2], S7G2
nxd_mdns	Azure RTOS NetX Duo mDNS/DNS-SD	S3A7, S5D9, S7G2
nxd_nat	Azure RTOS NetX Duo NAT	S5D9[2], S7G2
nxd_pop3	Azure RTOS NetX Duo POP3	S5D9[2], S7G2
nxd_ppp	Azure RTOS NetX Duo PPP	S5D9[2], S7G2[2]
nxd_smtp_client	Azure RTOS NetX Duo SMTP Client	S5D9[2], S7G2
nxd_snmp	Azure RTOS NetX Duo SNMP	S5D3[2], S5D5[2], S5D9[2], S7G2

[2] NetX and NetX Duo Applications are MCU-independent application layer protocols dependent on the NetX and Ethernet drivers. All MCUs on which NetX has been tested and verified support these protocols.

Module Name	SSP Feature	Supported Synergy MCU Groups
nxd_sntp_client	Azure RTOS NetX Duo SNTP Client	S5D9[2], S7G2
nxd_telnet_client	Azure RTOS NetX Duo Telnet Client	S5D9[2], S7G2
nxd_telnet_server	Azure RTOS NetX Duo Telnet Server	S5D9[2], S7G2
nxd_tftp_client	Azure RTOS NetX Duo TFTP Client	S5D9[2], S7G2
nxd_tftp_server	Azure RTOS NetX Duo TFTP Server	S5D9[2], S7G2
nxd_mqtt_client	Azure RTOS NetX Duo MQTT Client	S5D3, S5D5, S5D9, S7G2
nxd_tls_secure[3]	Azure RTOS NetX Duo TLS Secure	S5D3, S5D5, S5D9, S7G2
nxd_web_http_client	Azure RTOS NetX Duo Web HTTP1.1 Client	S5D5[2], S5D9, S7G2
	Azure RTOS NetX Duo Web HTTPS Client	S5D5, S5D9, S7G2
nxd_web_http_server	Azure RTOS NetX Duo Web HTTP1.1 Server	S5D9, S7G2
	Azure RTOS NetX Duo Web HTTPS Server	S5D9, S7G2
Tx	Azure RTOS ThreadX	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
Lx_nor	Azure RTOS LevelX NOR	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_storage	Azure RTOS USBX Device Class Mass Storage	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_hid	Azure RTOS USBX Device Class HID	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_device_class_cdc_acm	Azure RTOS USBX Device Class CDC-ACM	S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_cdc_acm	Azure RTOS USBX Host Class CDC-ACM	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_hid	Azure RTOS USBX Host Class HID	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_hub	Azure RTOS USBX Host HUB	S5D3, S5D5, S5D9, S7G2
ux_host_class_printer	Azure RTOS USBX Host Class Printer	S3A3, S3A7, S5D9, S7G2
ux_host_class_storage	Azure RTOS USBX Host Class Mass Storage	S3A1, S3A3, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_video	Azure RTOS USBX Host Video class	S5D9, S7G2

[4] NetX and NetX Duo Applications are MCU-independent application layer protocols dependent on the NetX and Ethernet drivers. All MCUs on which NetX has been tested and verified support these protocols.

[3] TLS v1.0 and v1.1 are deprecated from SSP and will be obsolete from next SSP release. Users are strongly recommended to migrate their projects to TLS v1.3 in SSP immediately.

9.4 Cryptographic Functions for Each MCU Supported in this Release

Function	S5D3, S5D5, S5D9, S7G2	S3A1, S3A3, S3A6, S3A7	S124, S128, S1JA
TRNG	Generate and read random number	Generate and read random number	Generate and read random number
AES	Encryption, decryption, Key Generation - wrapped keys	Encryption, decryption, Key Generation - wrapped keys	Encryption, decryption
AES Key Size	128-bit, 192-bit, 256-bit	128-bit, 256-bit	128-bit, 256-bit
AES Key Type	Plain text / raw key, wrapped key	Plain text / raw key, wrapped key	Plain text / raw key
AES Chaining Modes	ECB, CBC, CTR, GCM, XTS[6]	ECB, CBC, CTR, GCM, XTS	ECB, CBC, CTR
ARC4	Encryption, decryption	NA	NA
TDES	Encryption, decryption	NA	NA
TDES Key Size	192-bit	NA	NA
TDES Chaining Modes	ECB, CBC, CTR	NA	NA
RSA	Signature Generation, Signature Verification, Public-key Encryption, Private-key Decryption, Key Generation - plain text and wrapped keys	NA	NA
RSA Key Size	1024-bit, 2048-bit	NA	NA
RSA Key Type	Plain text / raw key, Wrapped key	NA	NA
Key Installation	AES, ECC, RSA keys	AES keys	NA
ECC	Key Generation – plain text and wrapped keys, Scalar Multiplication, ECDSA – Signature Generation, ECDSA – Signature Verification	NA	NA
ECC Key Size (in bits)	192-bit, 224-bit, 256-bit, and 384-bit	NA	NA
ECC Key Type	Plain text / raw keys and wrapped keys	NA	NA
DSA	Signature Generation, Signature Verification	NA	NA
DSA Key Size	(1024, 160)-bit, (2048, 224)-bit, (2048, 256)-bit	NA	NA
HASH	SHA1, SHA224, SHA256, MD5	NA	NA

[6] XTS is supported for 128-bit and 256-bit keys only.

9.5 Experimental Modules Supported in this Release

Modules that have not been tested on the MCUs have been classified as experimental modules and are listed in the following table. These experimental modules are currently not supported by Synergy Configuration tools and use of these modules in customer projects is not supported by Renesas at this time.

Experimental Modules		
Module Name	**SSP Feature**	**Supported Synergy MCU Groups**
ux_device_class_cdc_ecm	Azure RTOS USBX Device Class CDC-ECM	S124, S3A3, S3A7, S5D9, S7G2
ux_device_class_rndis	Azure RTOS USBX Device Class RNDIS	S124, S3A3, S3A7, S5D9, S7G2
ux_host_class_gser	Azure RTOS USBX Host Class Generic Serial	S3A3, S3A7, S5D9, S7G2
ux_host_class_prolific	Azure RTOS USBX Host Class Prolific	S3A3, S3A7, S5D9, S7G2
ux_host_class_swar	Azure RTOS USBX Host Class Swar	S3A3, S3A7, S5D9, S7G2
ux_network_driver	Azure RTOS USBX Network Driver	S124, S3A3, S3A7, S5D9, S7G2
ux_device_class_pima	Azure RTOS USBX PIMA Device Class	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_host_class_pima	Azure RTOS USBX PIMA Host Class	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2
ux_pictbridge	Azure RTOS Pictbridge Class	S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2

10. Additional Technical Notes

General information

- General information, FAQs and online technical support for the Renesas Synergy™ Platform is available at the Renesas Engineering Community at https://community.renesas.com/mcu-mpu/embedded-system-platform/.
- Additional technical information, including informative papers and articles on SSP and Synergy can be found at Synergy Knowledge Base, www.renesas.com/synergy/knowledgebase.

For specific requests

You can also get ticket support at MyRenesas at https://www.renesas.com/myrenesas. To open a ticket:

1. Log in or register a new account here to access the information.
2. Click on the “support request” link.
   This opens the Knowledge base page.
3. Click on “SUBMIT A TICKET” option at the top right portion of the page.

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

Synergy Platform MCUs	Renesas Synergy™ Platform MCUs
Synergy Software Package	Renesas Synergy™ Software Package (SSP)
Software add-ons	Renesas Synergy™ Software Add-Ons
SSP Components	Synergy Software Package (SSP) Components
MCU Components	Components of Synergy MCUs
Kits	Renesas Synergy™ Kits
Partner projects	Renesas Synergy™ Partner Projects
Self-service support resources:	Renesas Synergy™ Support | Renesas
Knowledgebase	Renesas Synergy | Renesas Customer Hub
Synergy Community	Renesas Synergy™ Platform - Renesas Community
Training	Academy | Renesas Synergy™
Videos	Renesas Synergy™ Platform - YouTube

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.04.24	-	Preliminary draft
1.10	Mar.11.24	-	Updated for Friends and Family release
1.11	Mar.18.24	-	Added latest platform installer graphic. Updated latest fixed issue.

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