

| REVISIONS | | | | |
|-----------|-----|-----------------|------------|-----------|
| DCN | REV | DESCRIPTION | DATE | CHANGE BY |
| | 1.0 | INITIAL RELEASE | 2009-12-05 | T. TRAN |
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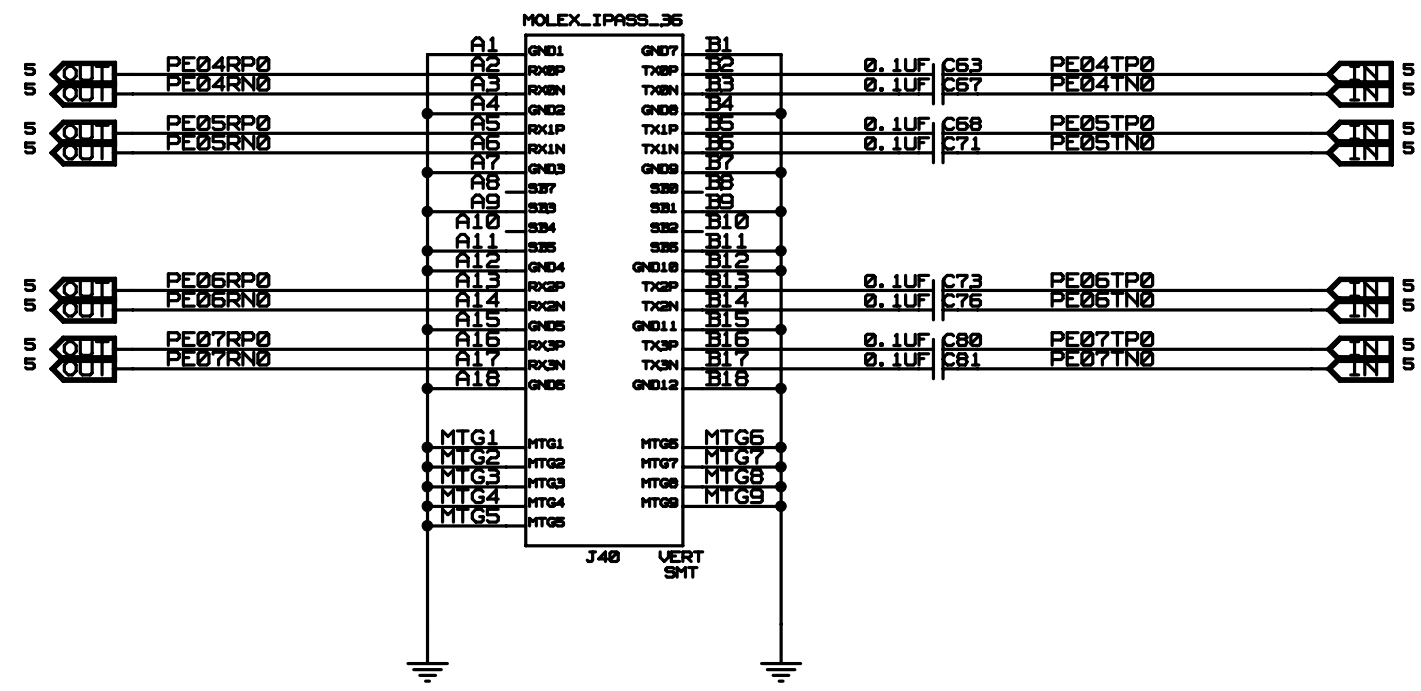
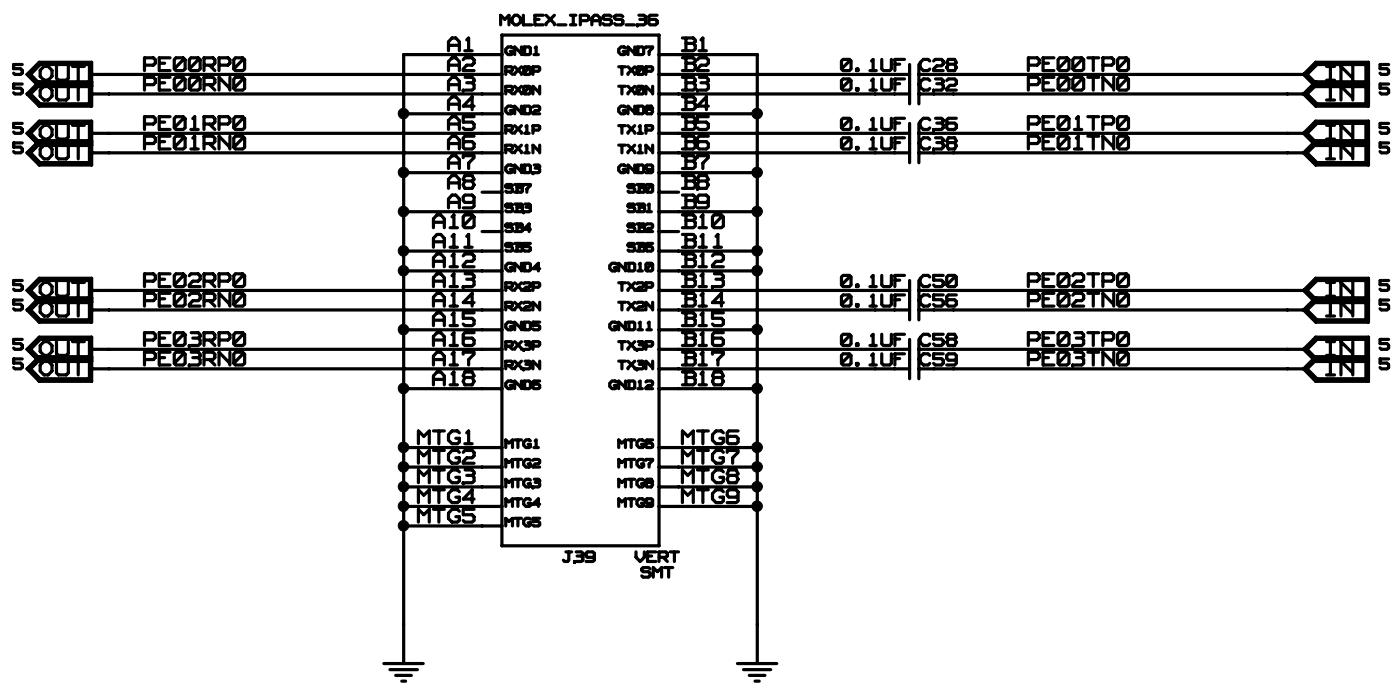
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| TITLE EB-LOGAN-19 | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:37:19 2010 | | | SHEET 1 OF 41 |



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| SAS CONNECTOR PORTS 0-7 | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:25 2010 | | | SHEET 2 OF 41 |

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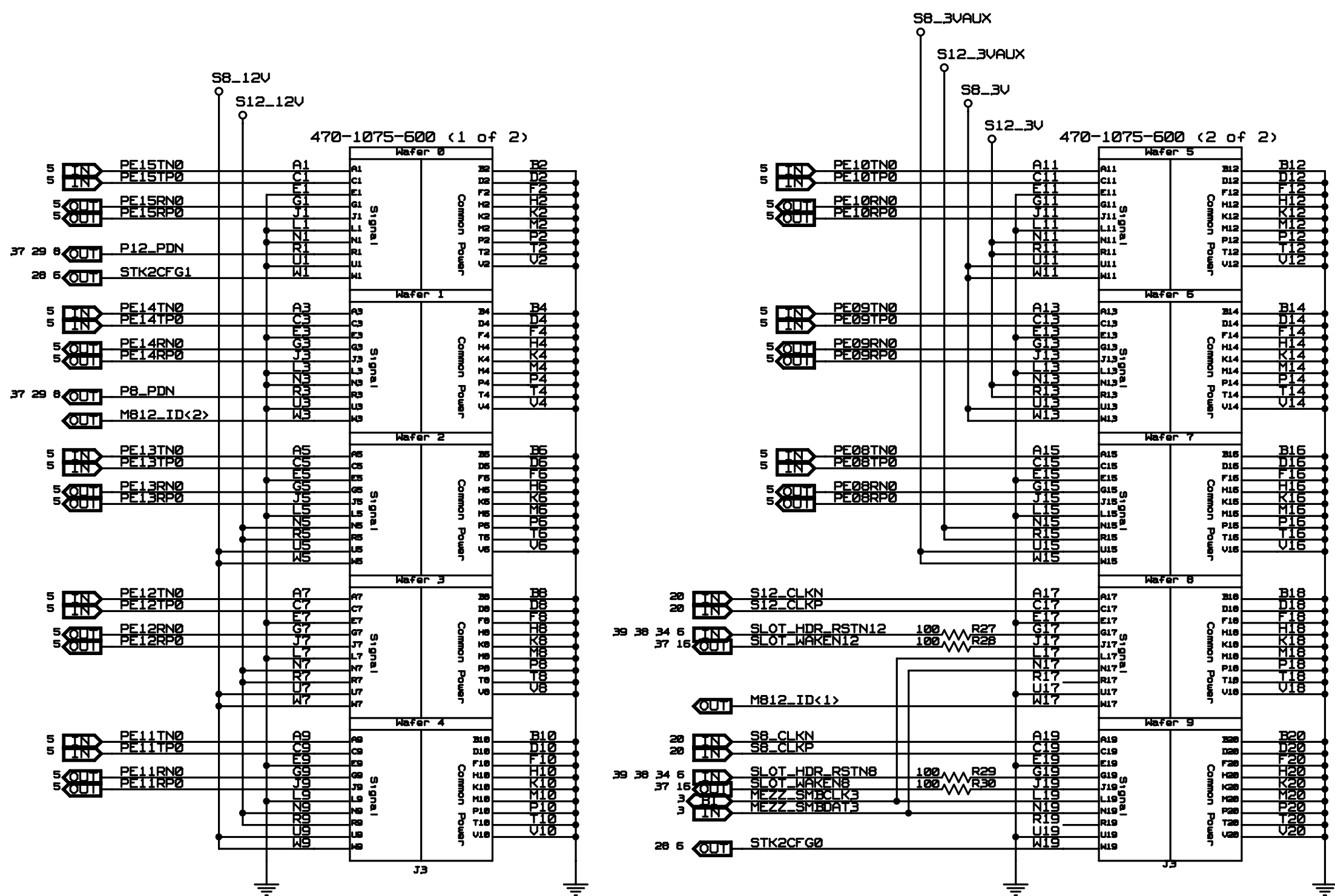
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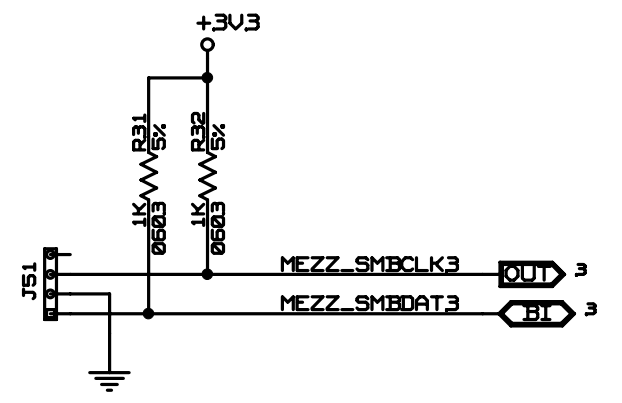
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A

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STK2CFG1 & STK2CFG0 SET BY MEZZ CARDS
 X8 - STK2CFG1 = 0, STK2CFG0 = 0
 X4 - STK2CFG1 = 0, STK2CFG0 = 1



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| TITLE EB-LOGAN-19 | | | |
| MEZZANINE CONNECTOR PORTS 8/12 | | | |
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| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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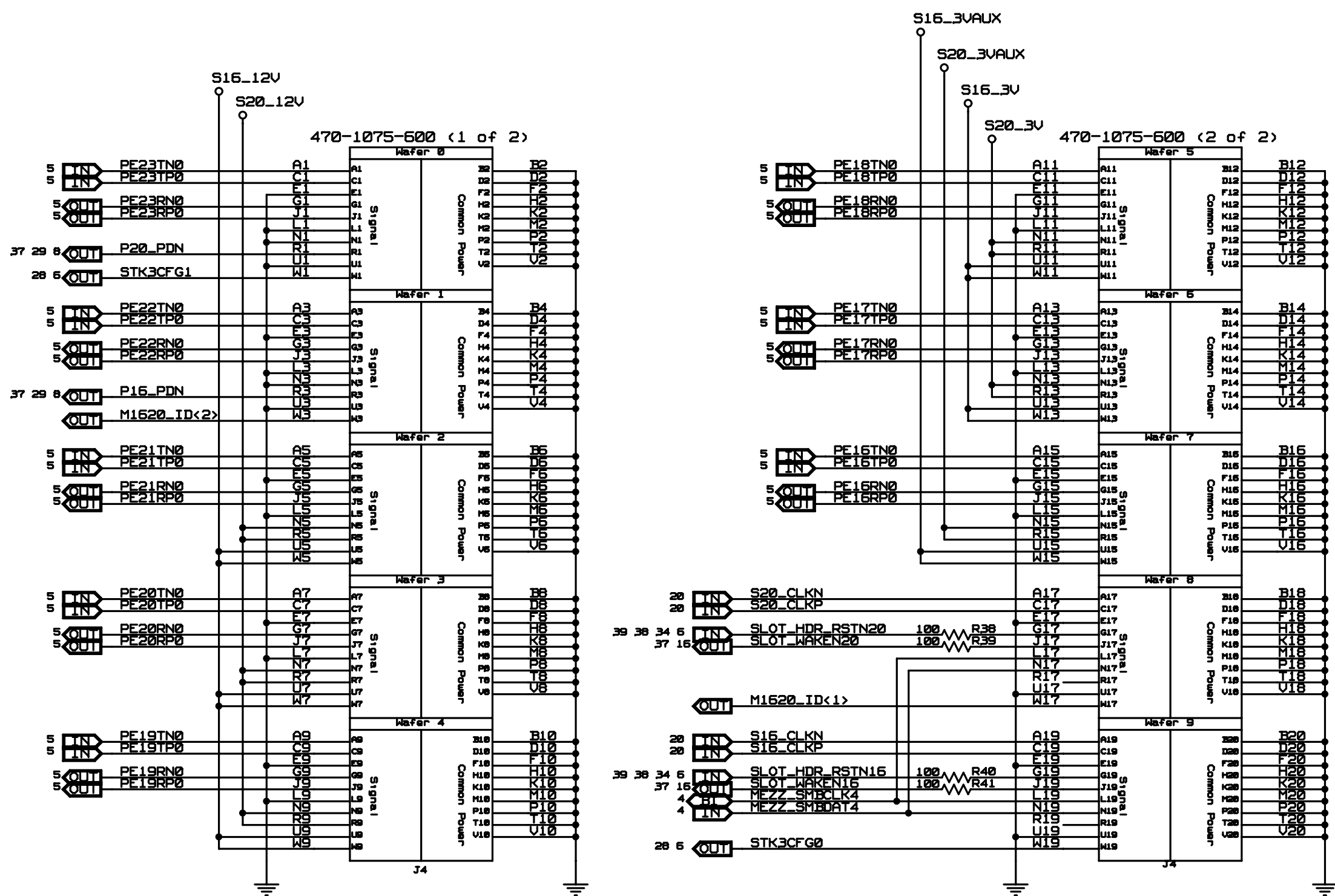
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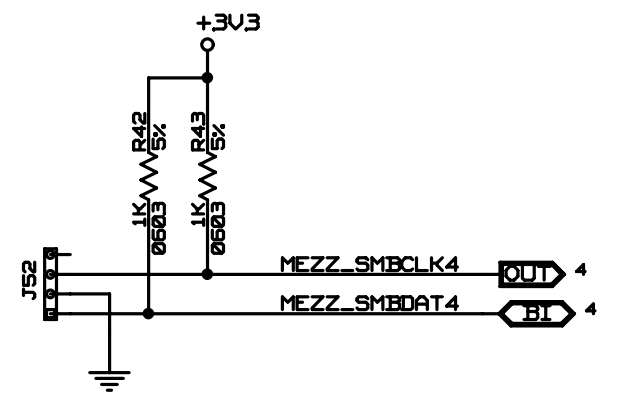
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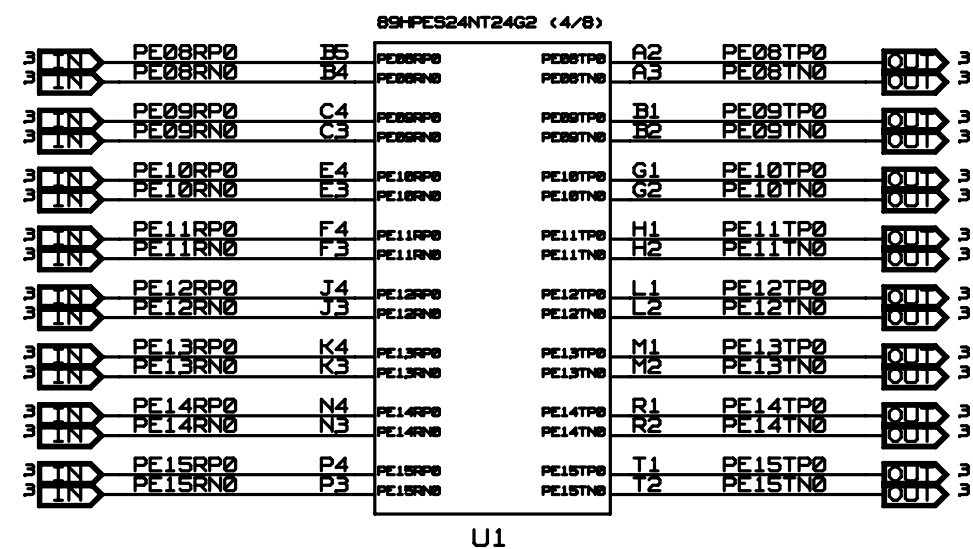
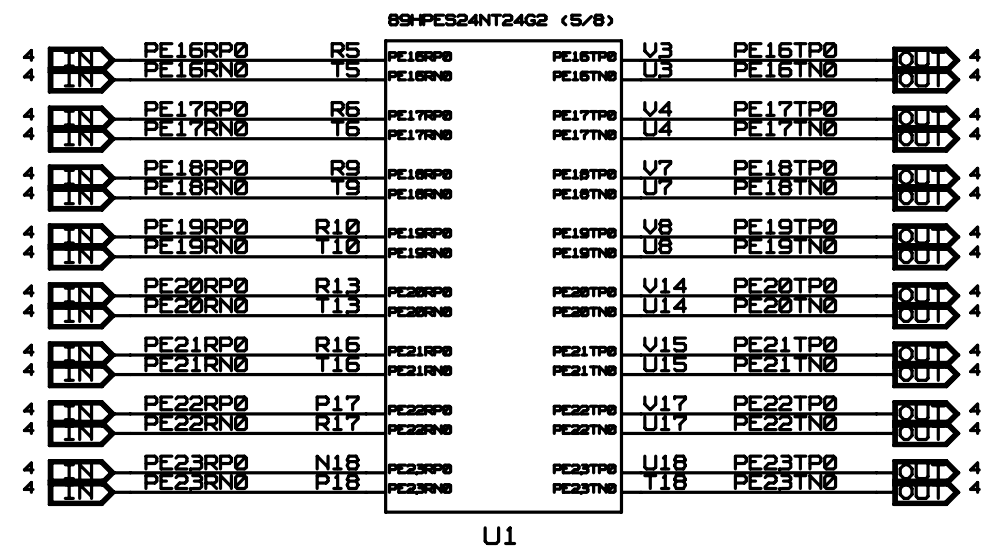
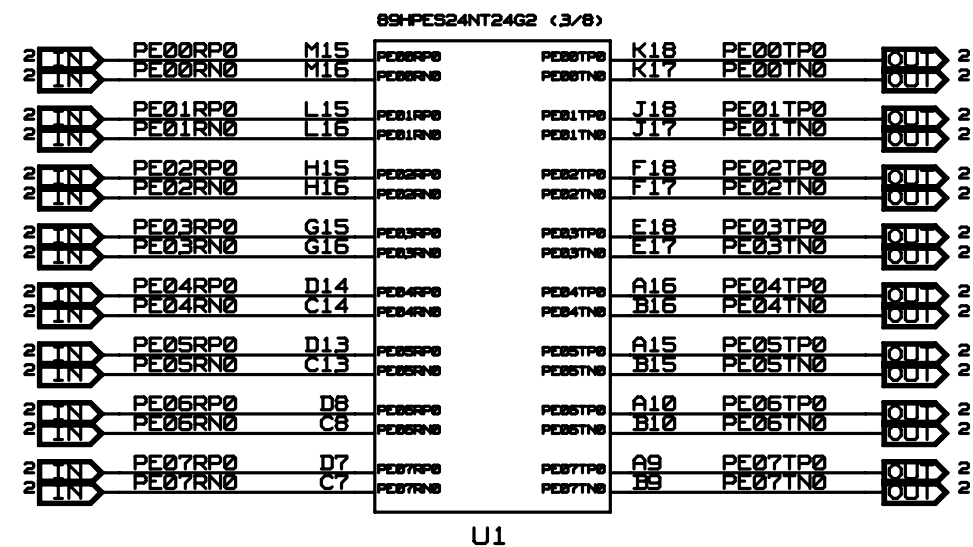


STK3CFG1 & STK3CFG0 SET BY MEZZ CARDS
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 X4 - STK3CFG1 = 0, STK3CFG0 = 1



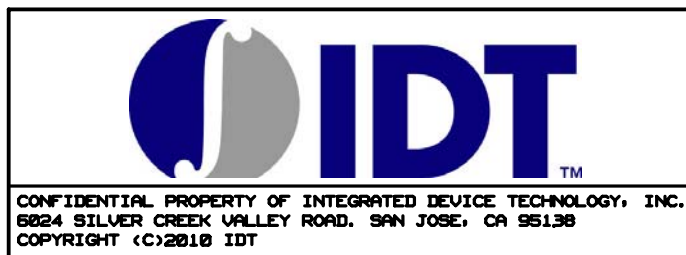
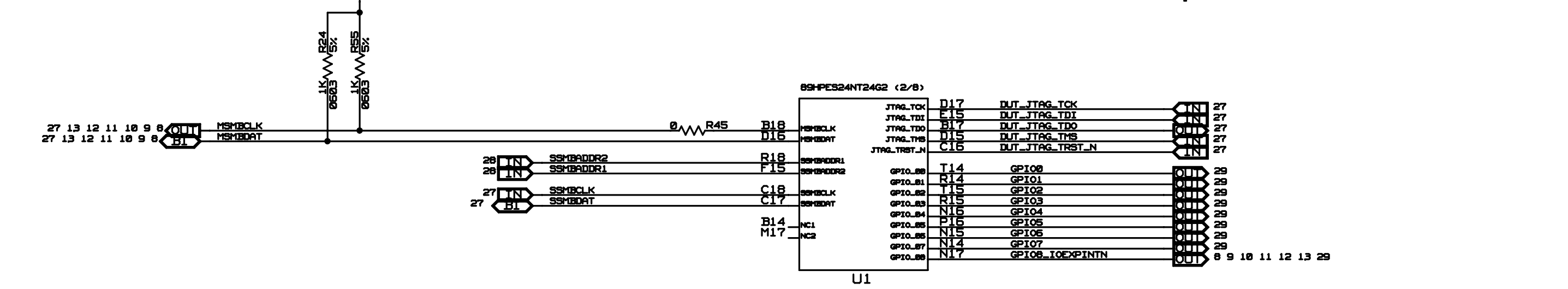
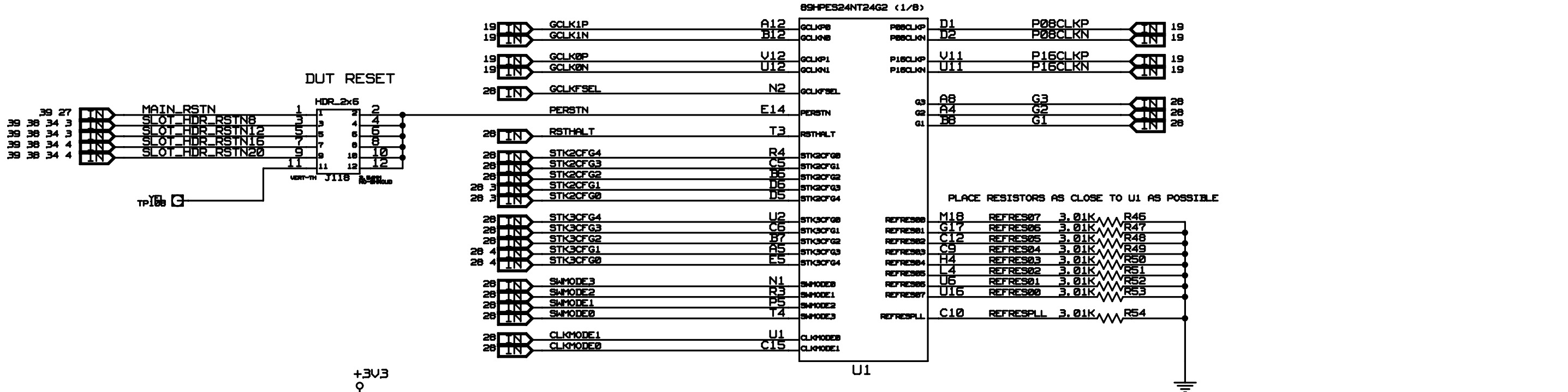
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| TITLE EB-LOGAN-19 | | | |
| MEZZANINE CONNECTOR PORTS 16/20 | | | |
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| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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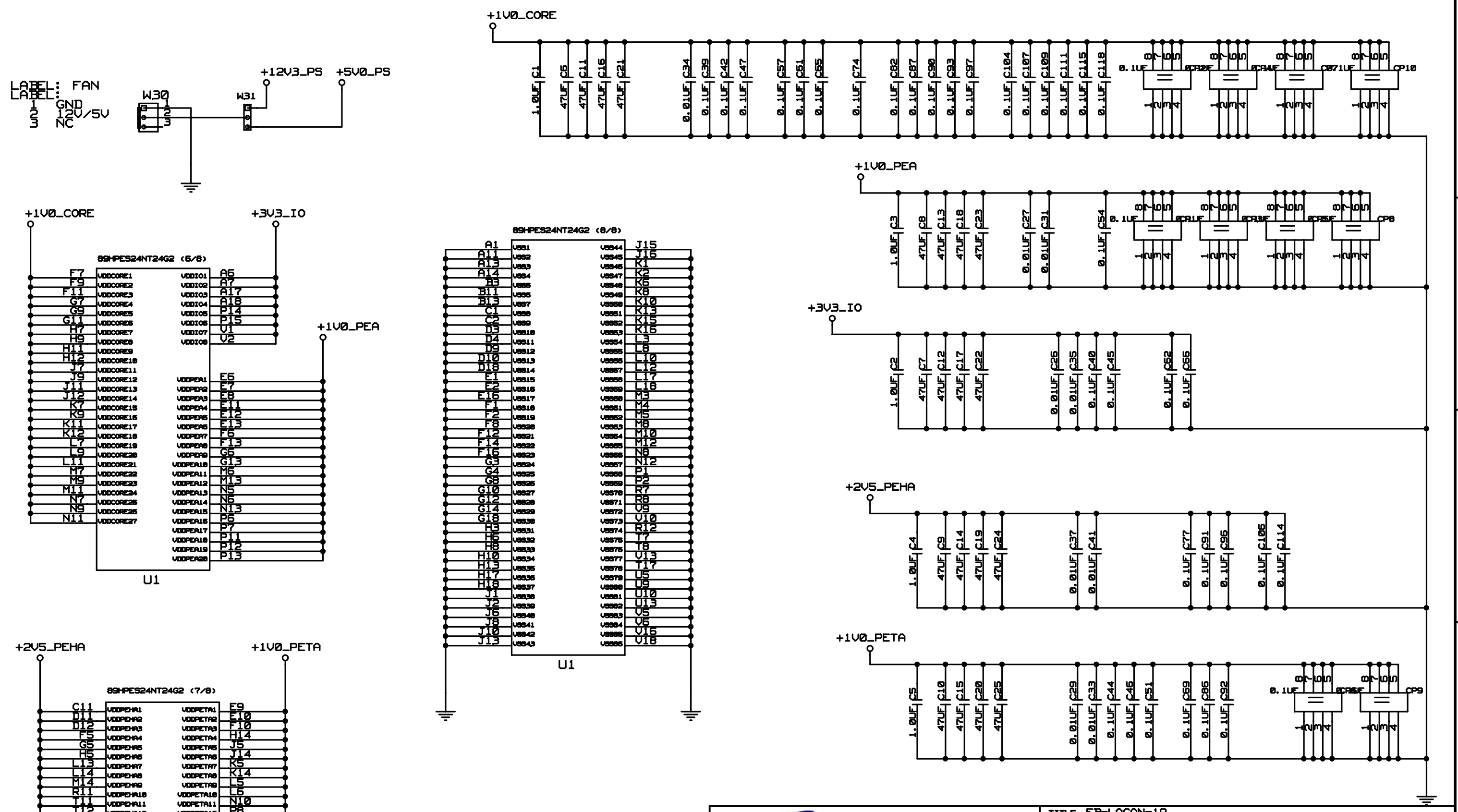
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| TITLE EB-LOGAN-19 | | | |
| 24NT24G2 - SERDES | | | |
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| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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| TITLE EB-LOGAN-19 | | | |
| 24NT24G2 - CLK, CONFIG, GPIO | | | |
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LABEL: FAN
 LABEL: FAN
 WND
 Z1 GND
 Z2 V/5V



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| 24NT24G2 - POWER | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
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| Tue Apr 20 12:38:33 2010 | | | SHEET 7 OF 41 |

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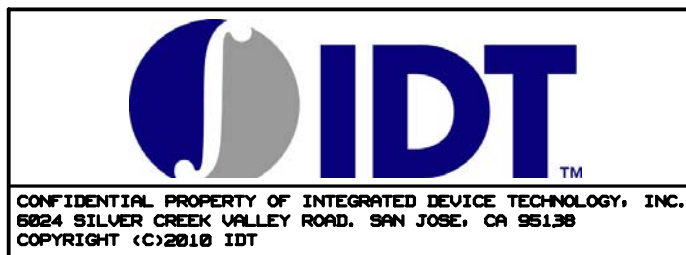
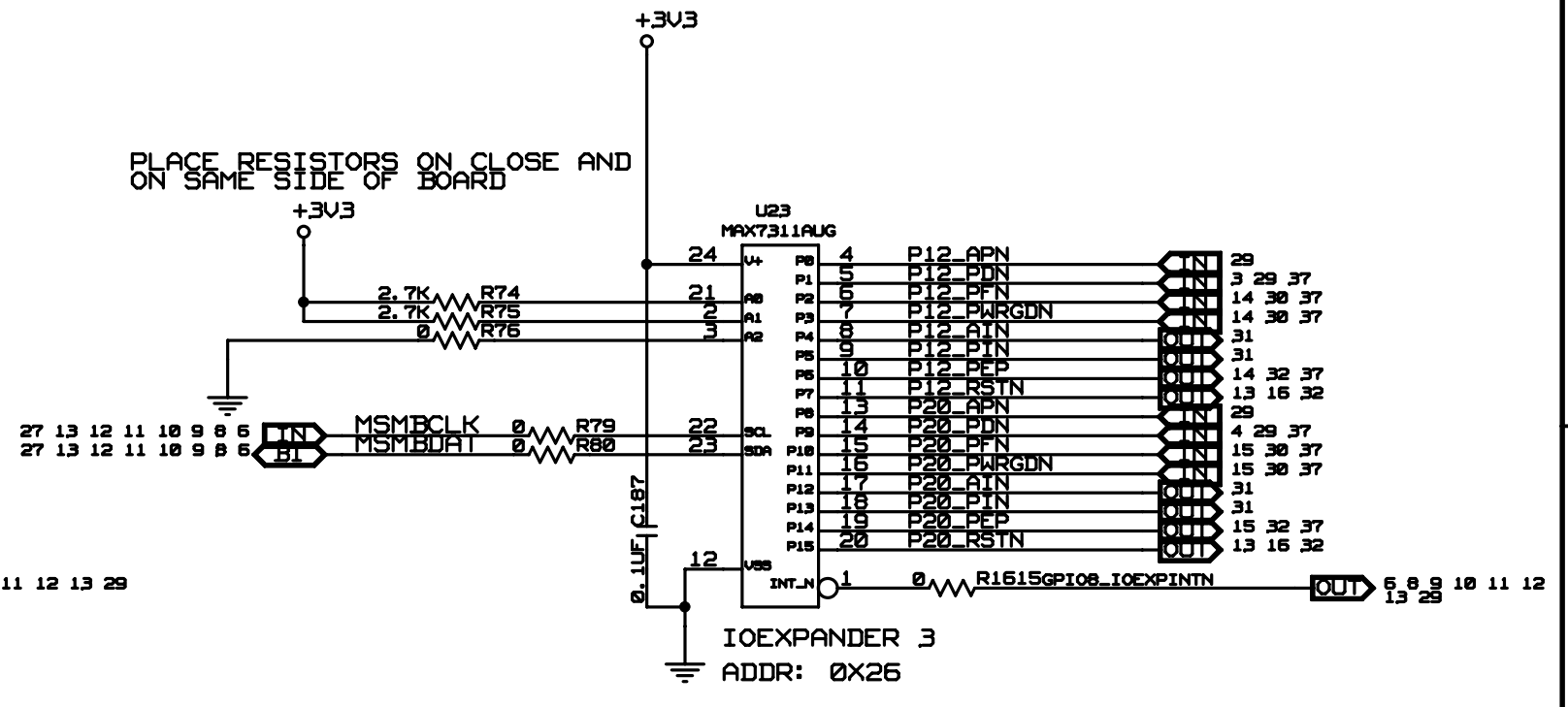
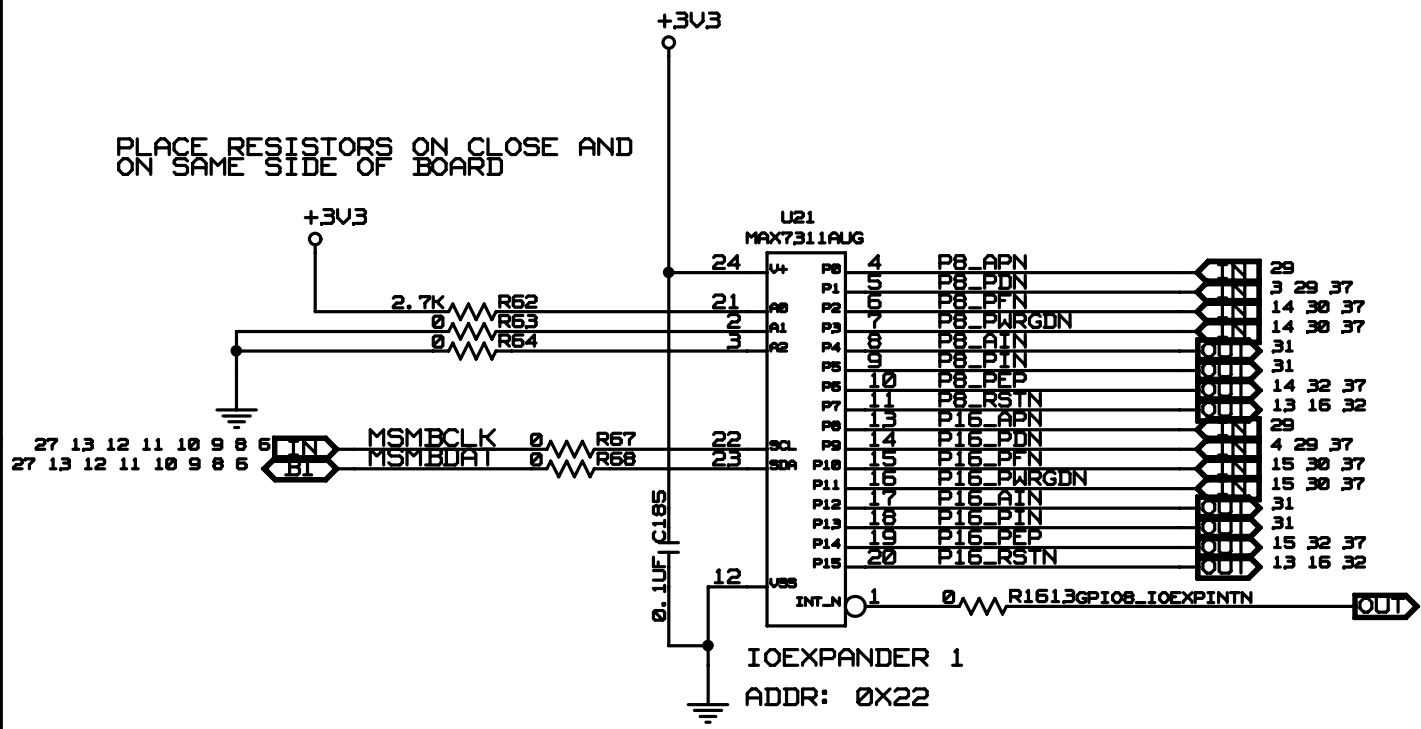
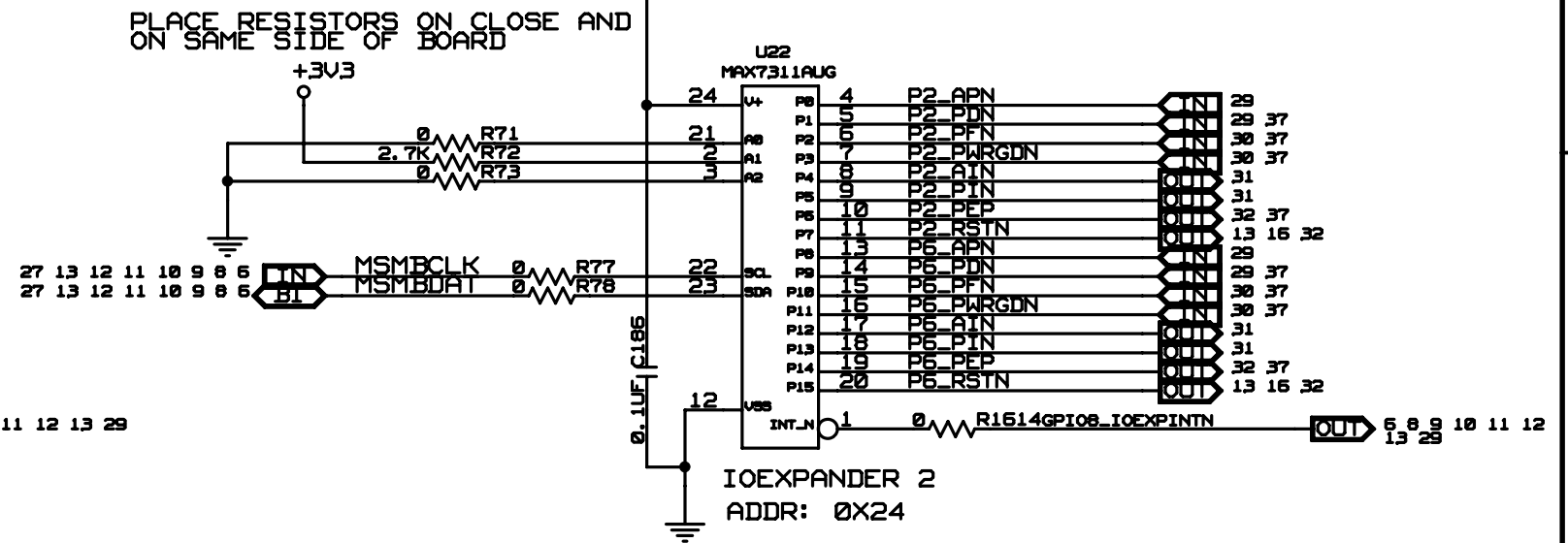
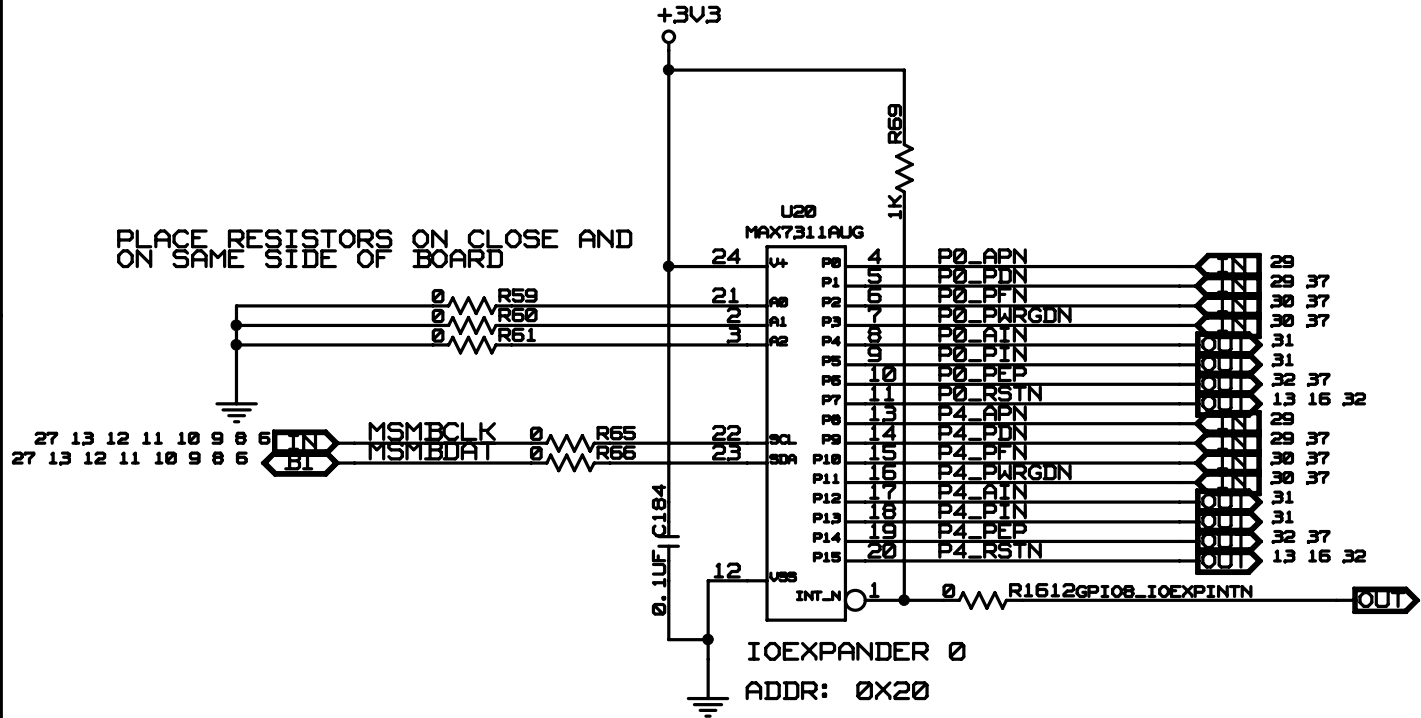
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| IOEXPANDER 0-3 | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
| AUTHOR | | CHECKED BY | |
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| Tue Apr 20 12:38:33 2010 | | | SHEET 8 OF 41 |

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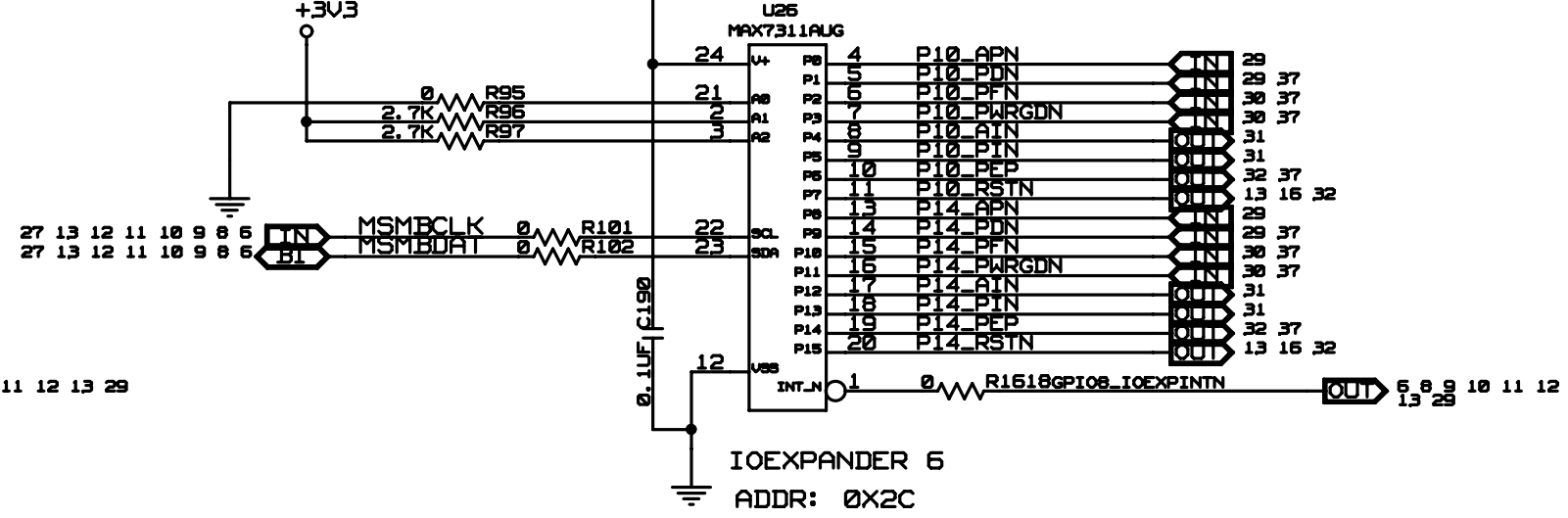
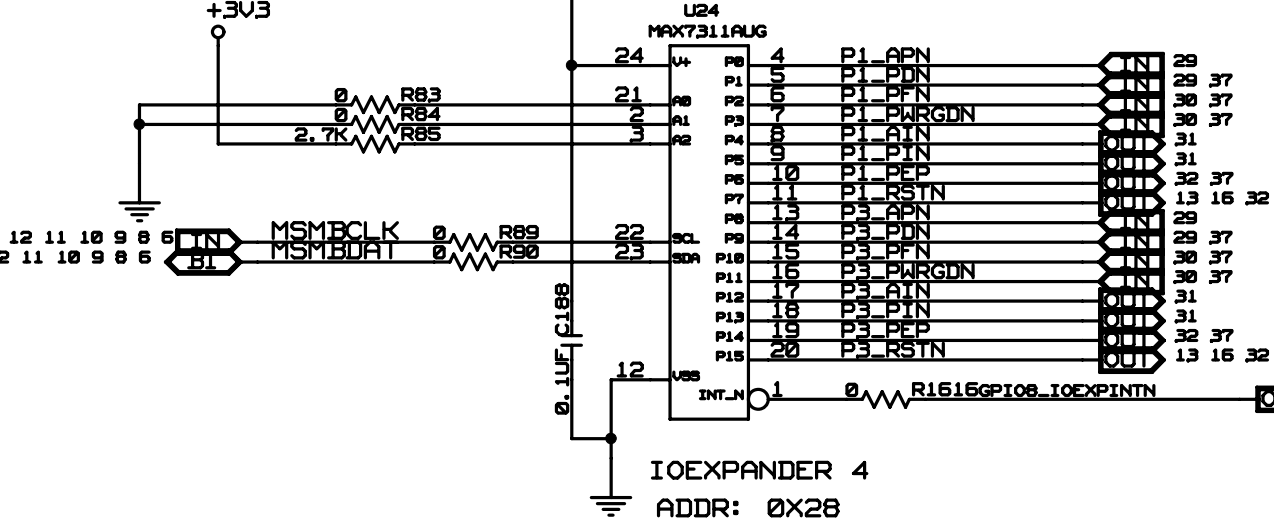
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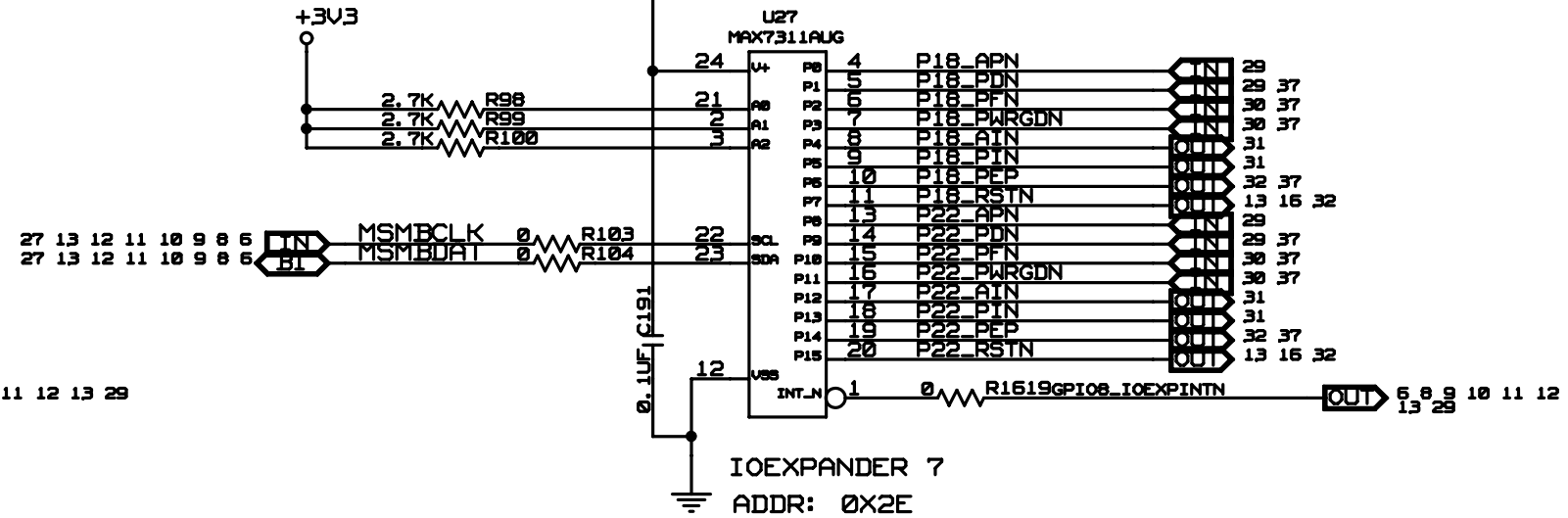
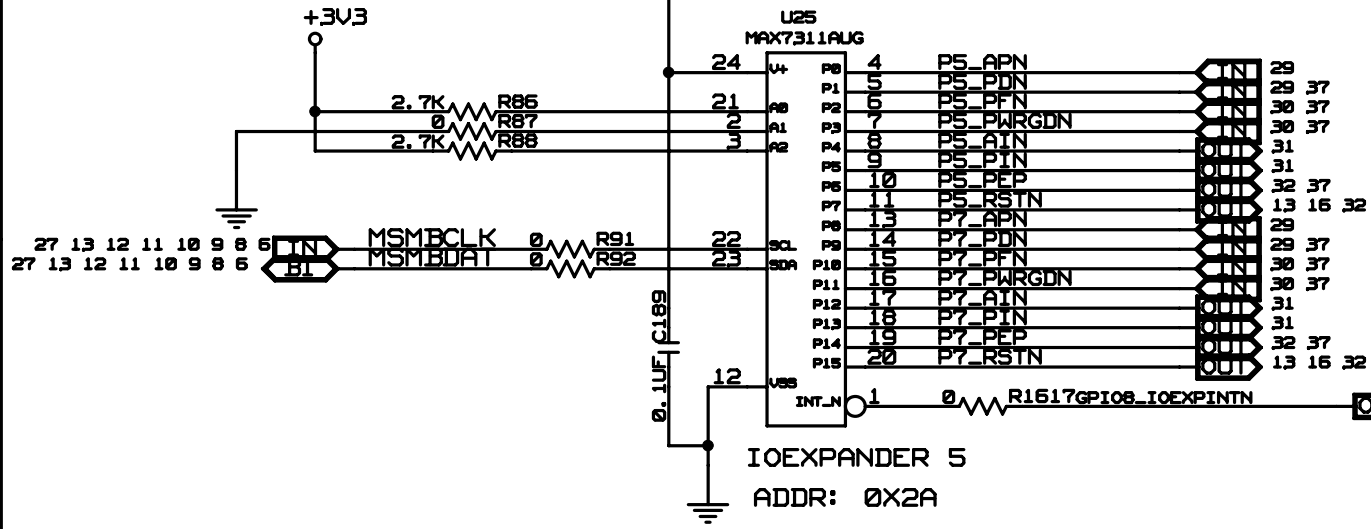
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



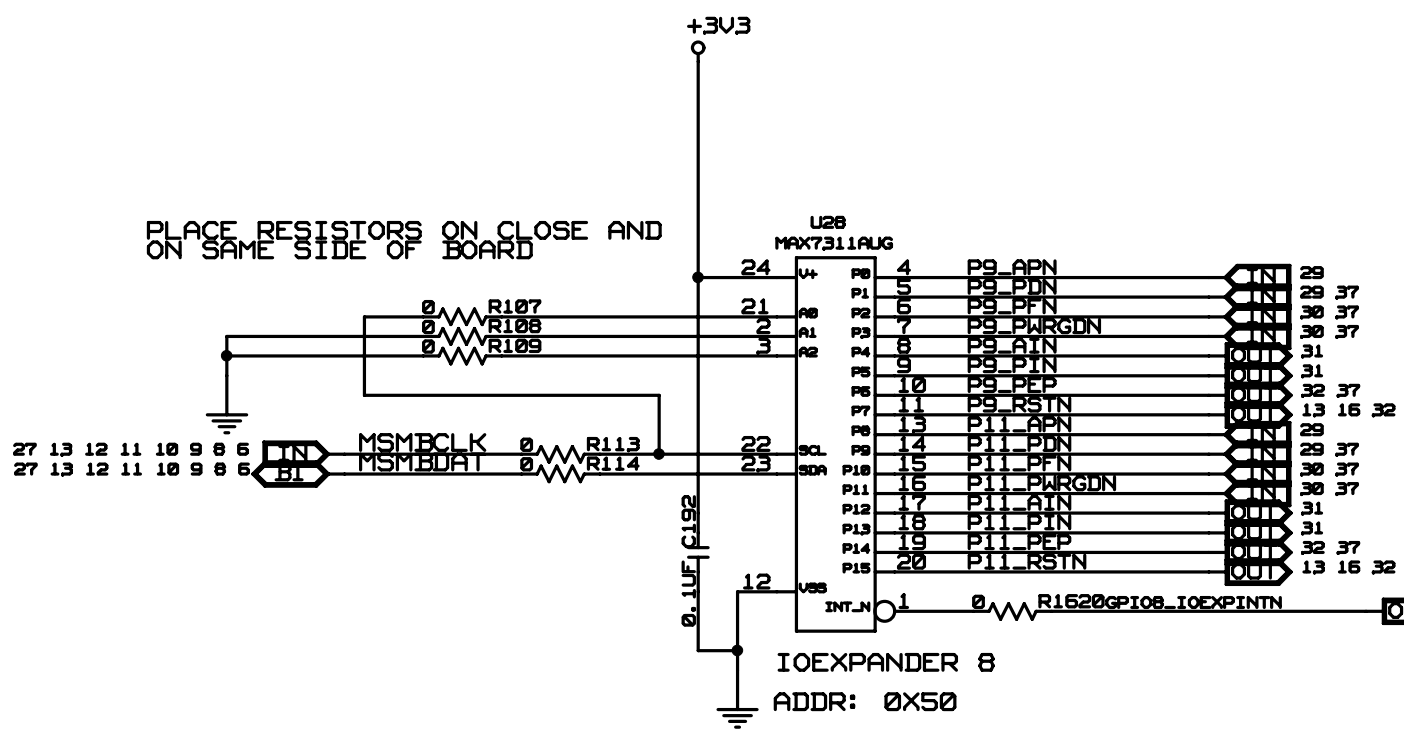
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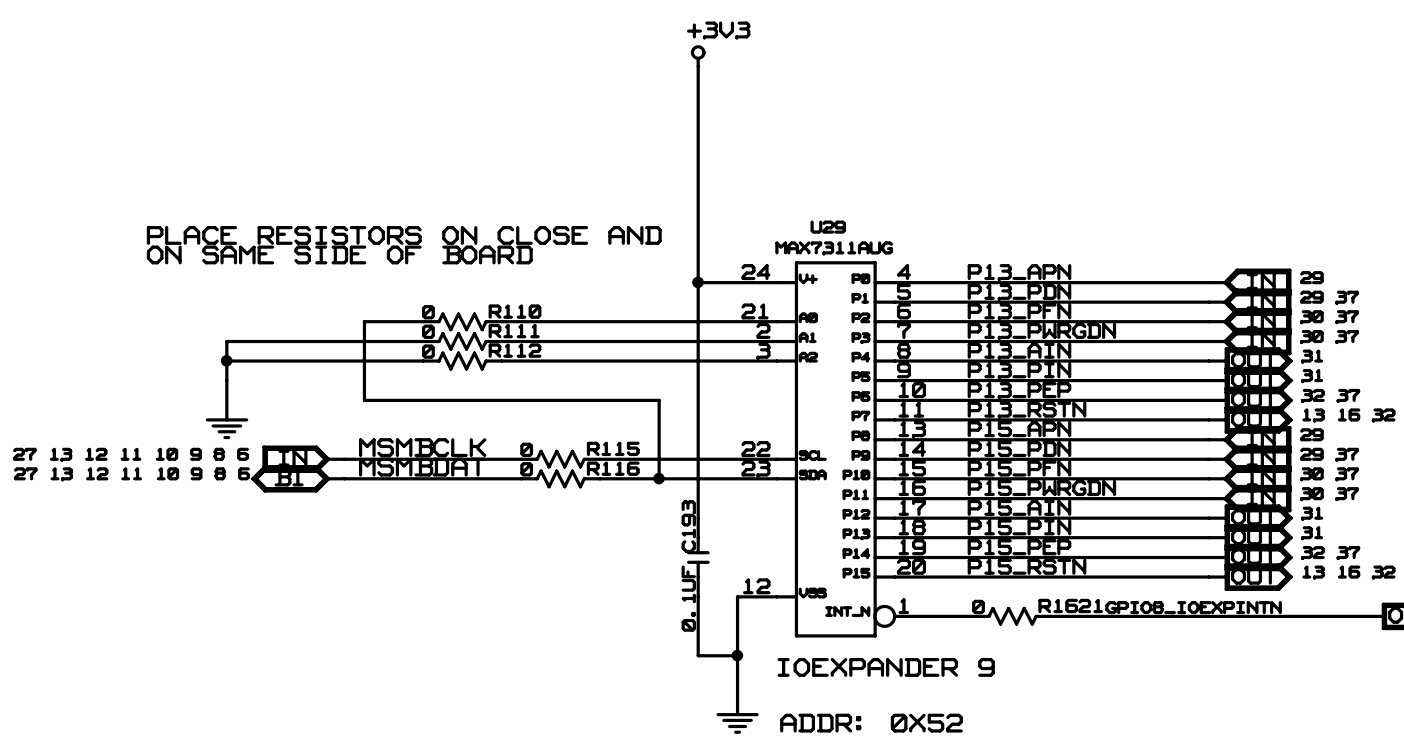
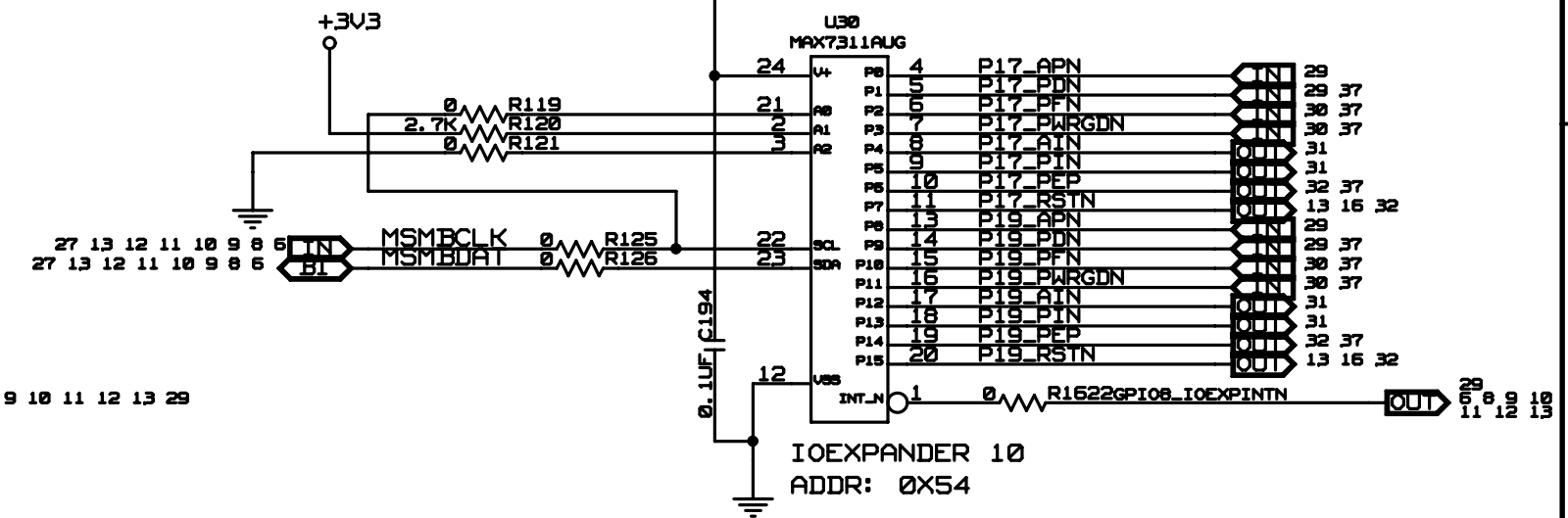


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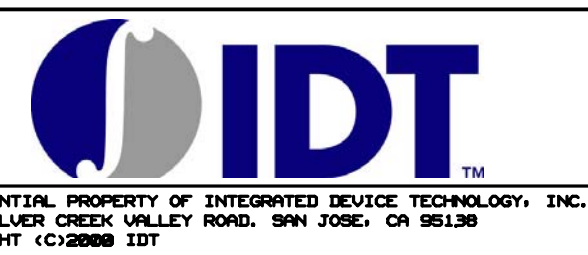
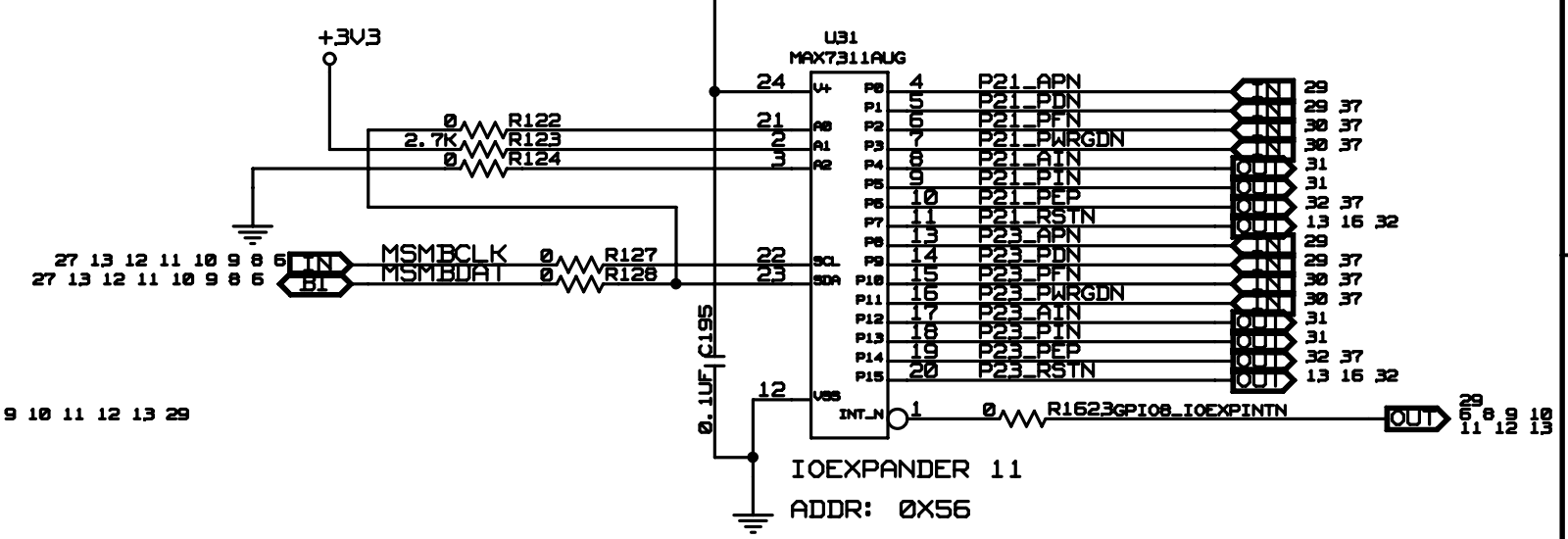
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| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
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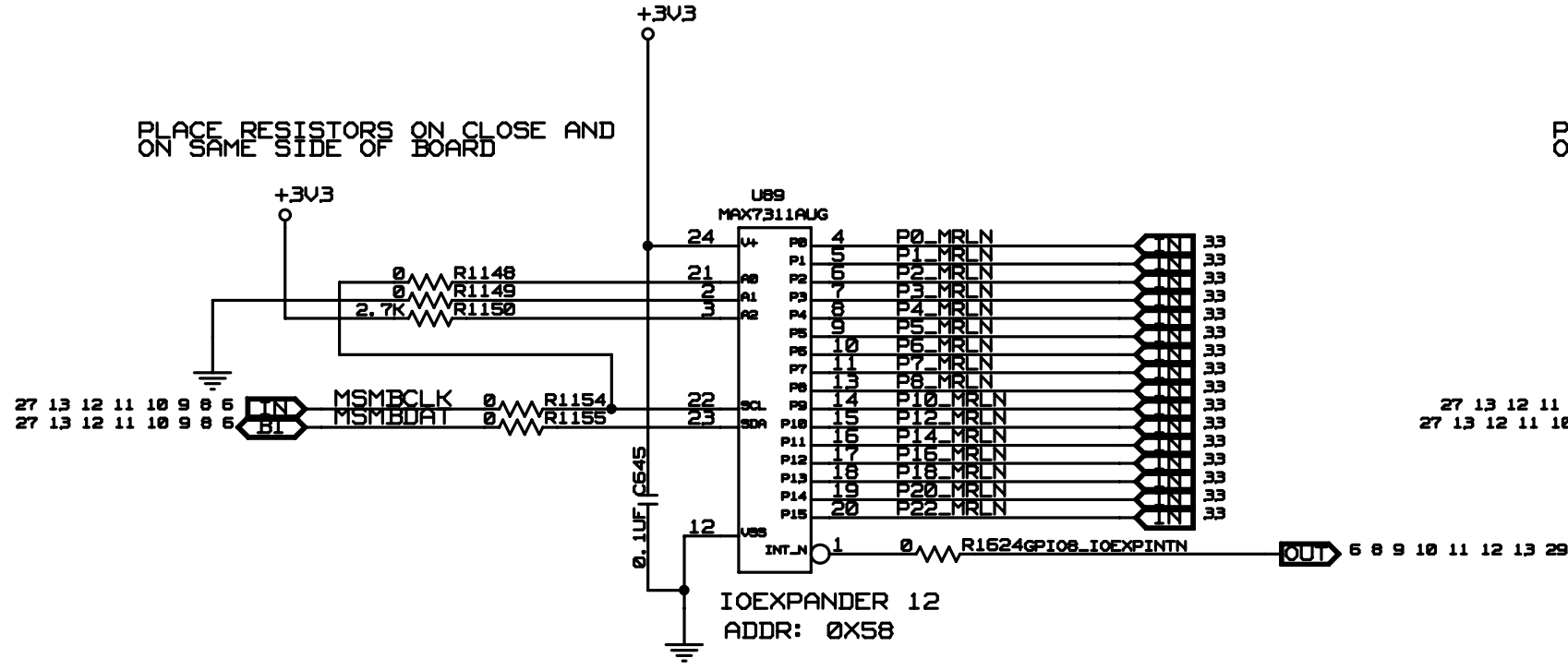


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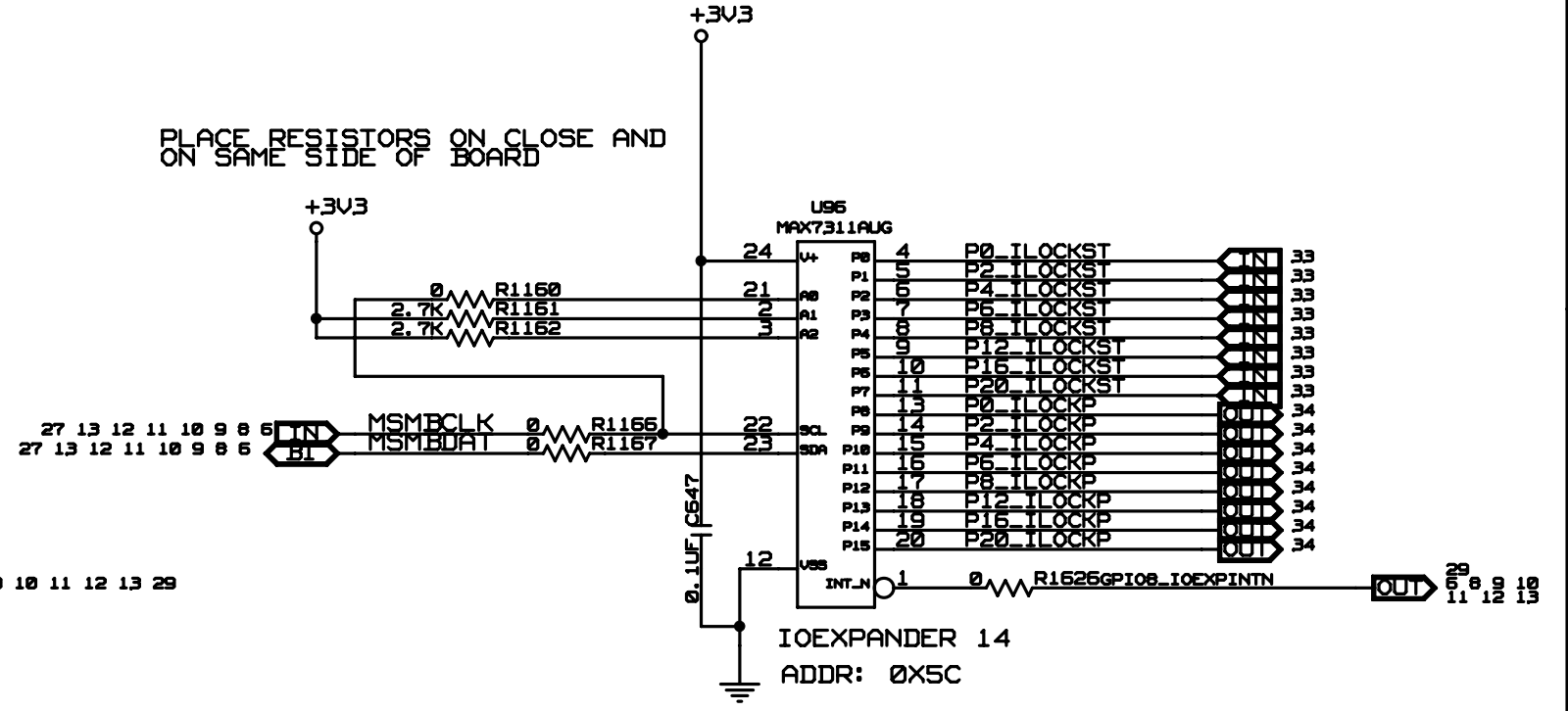


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| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
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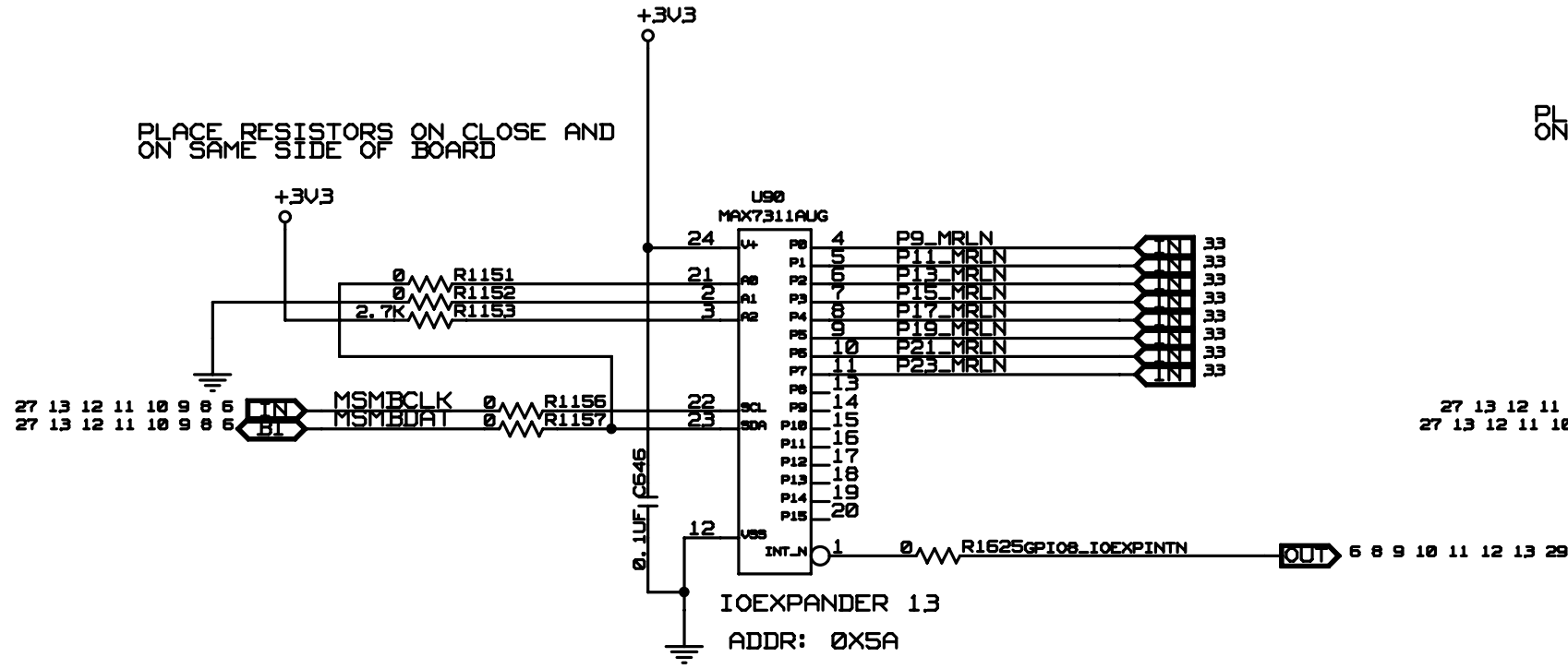
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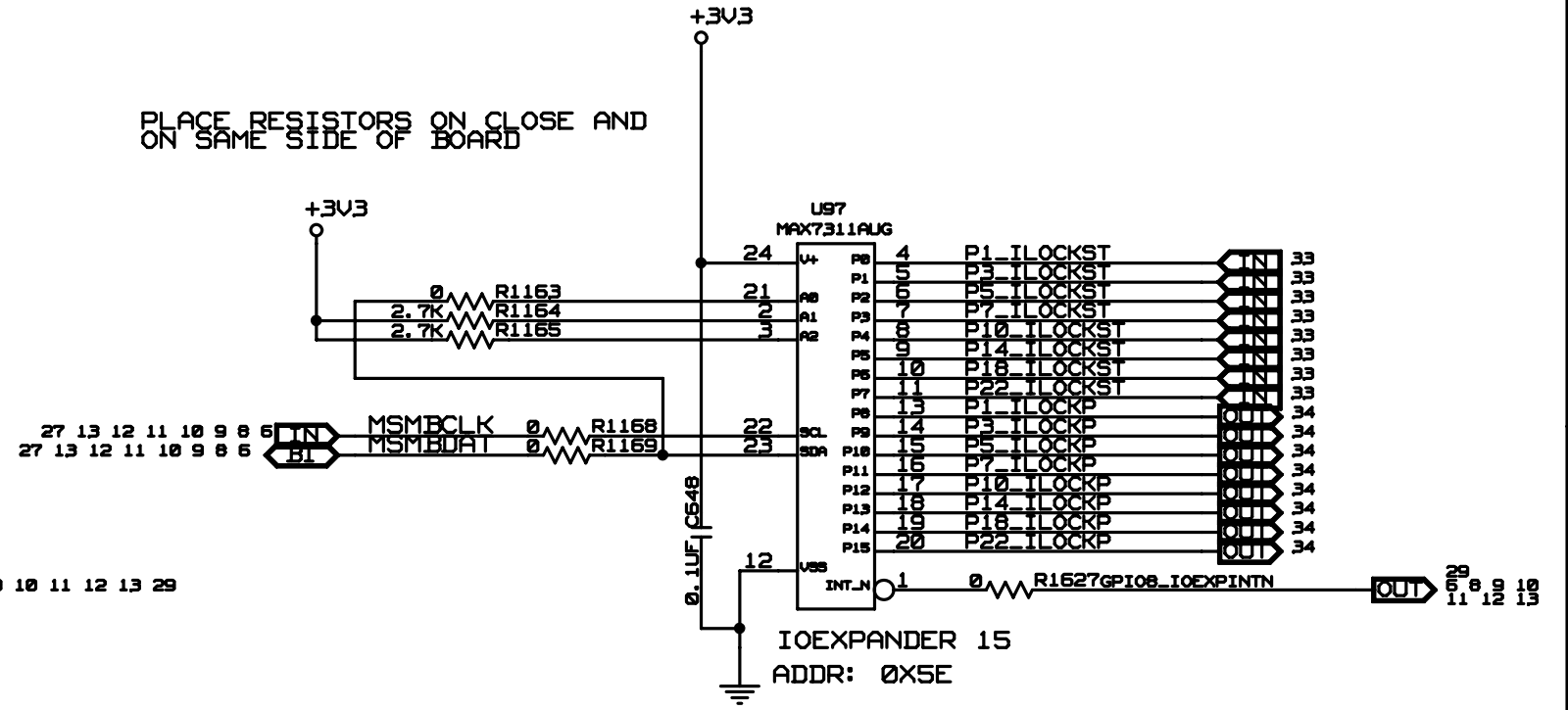
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



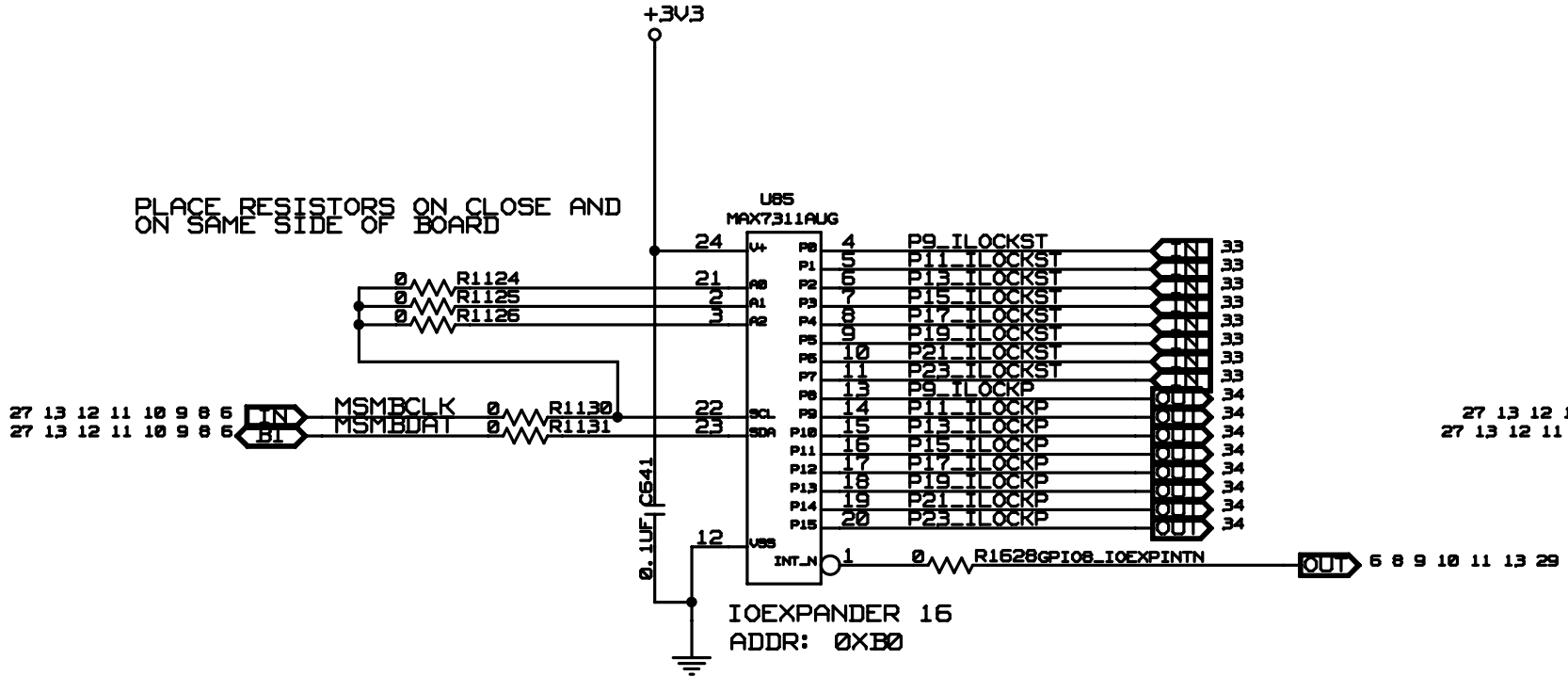
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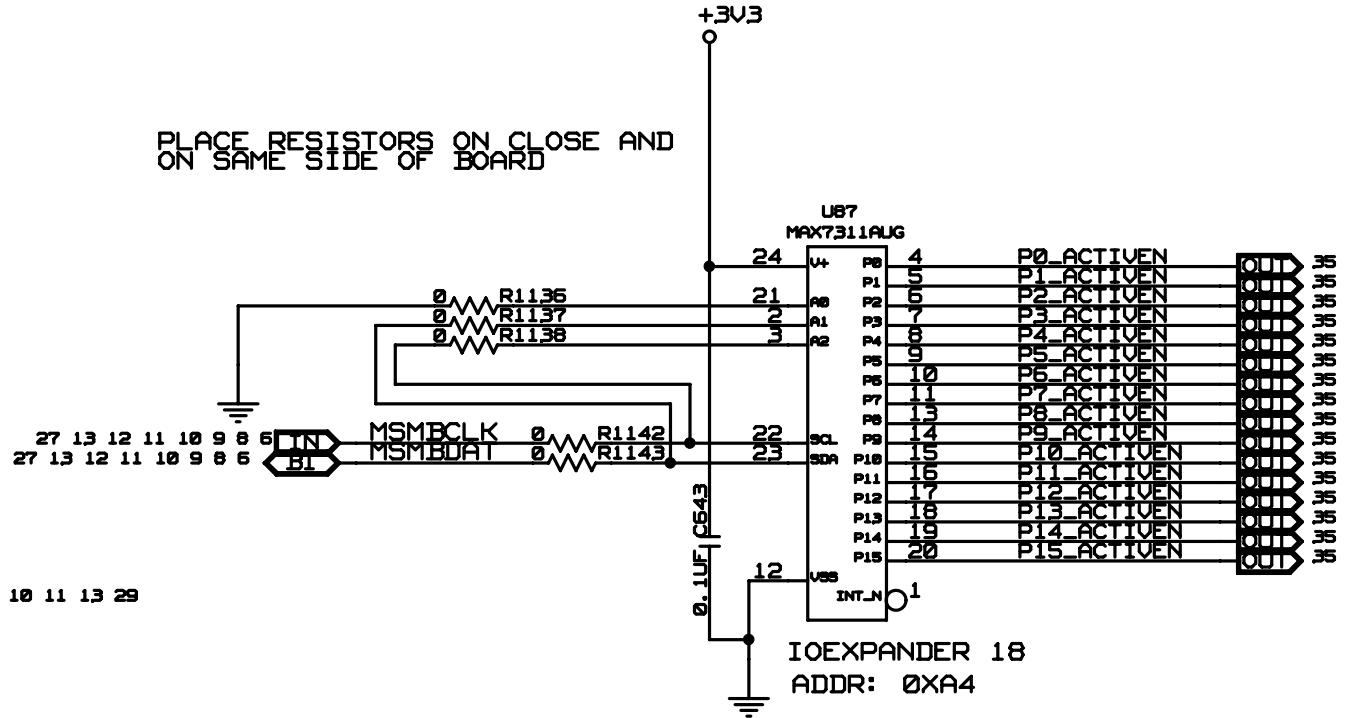
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| TITLE EB-LOGAN-19 | | | |
| IOEXPANDER 12-15 | | | |
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| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
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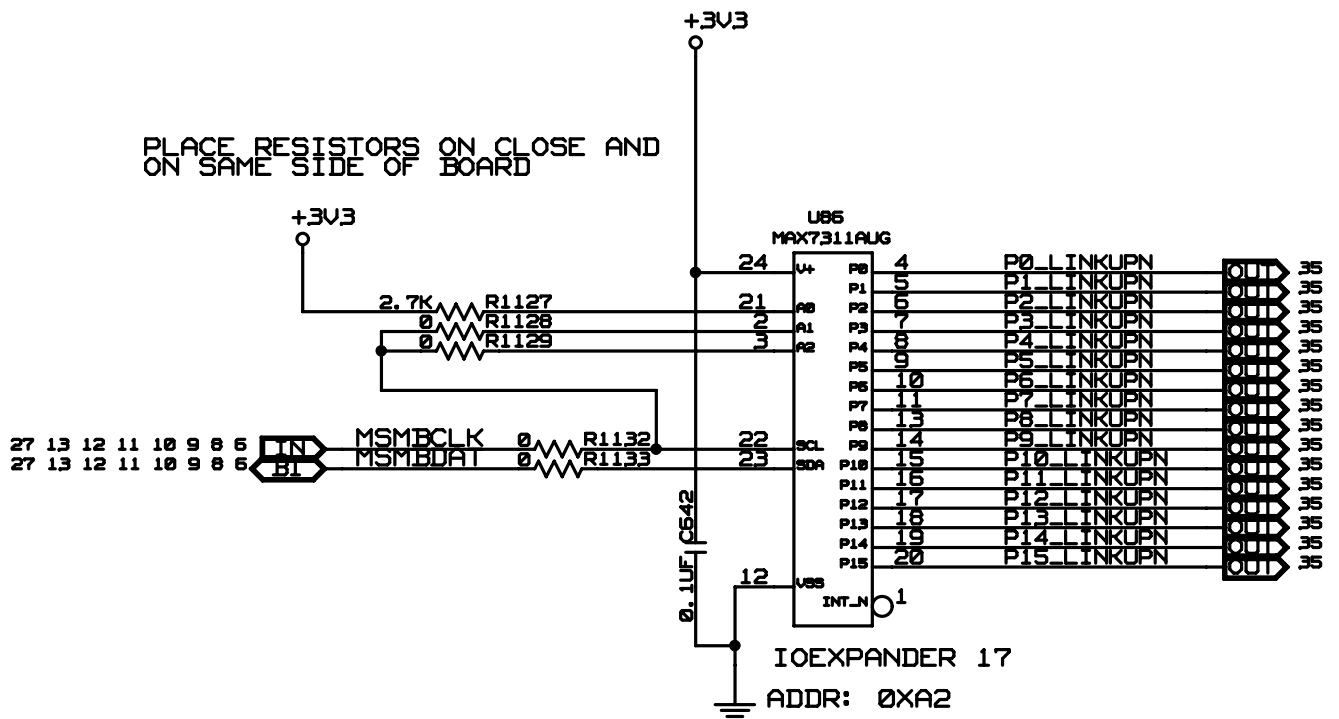
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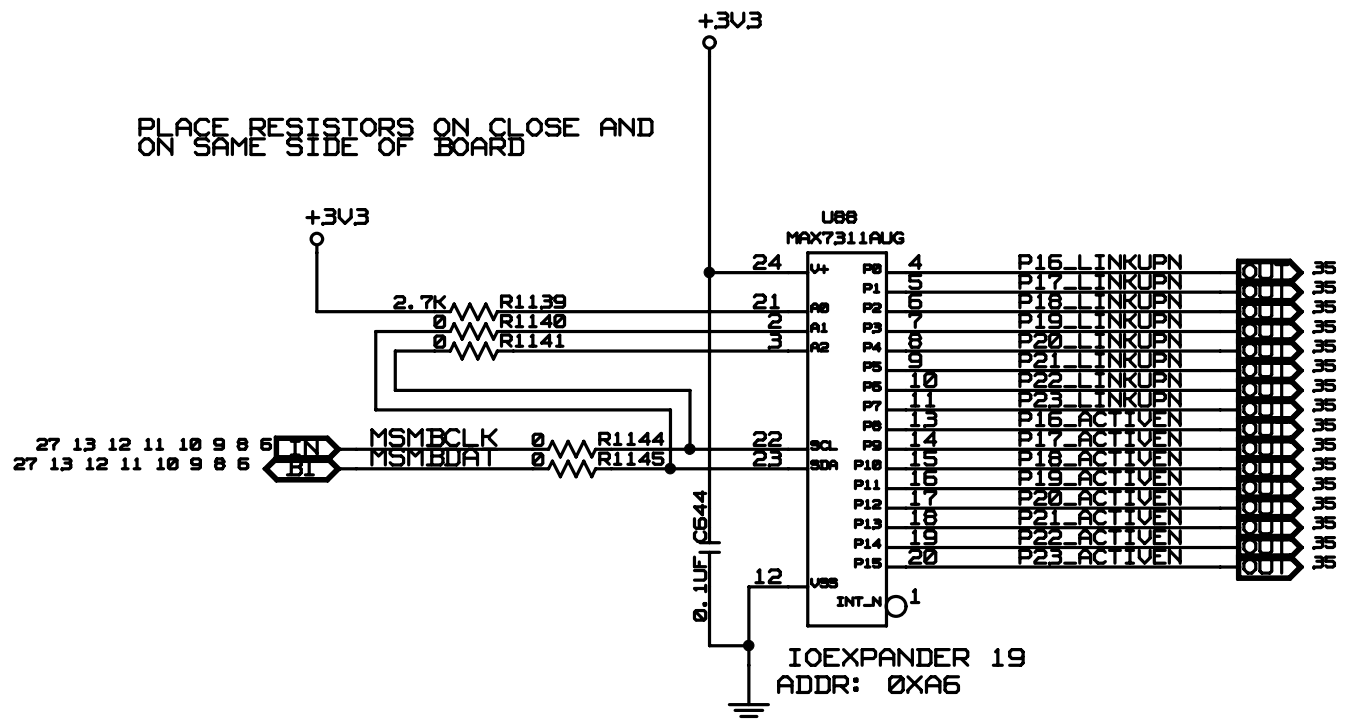
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



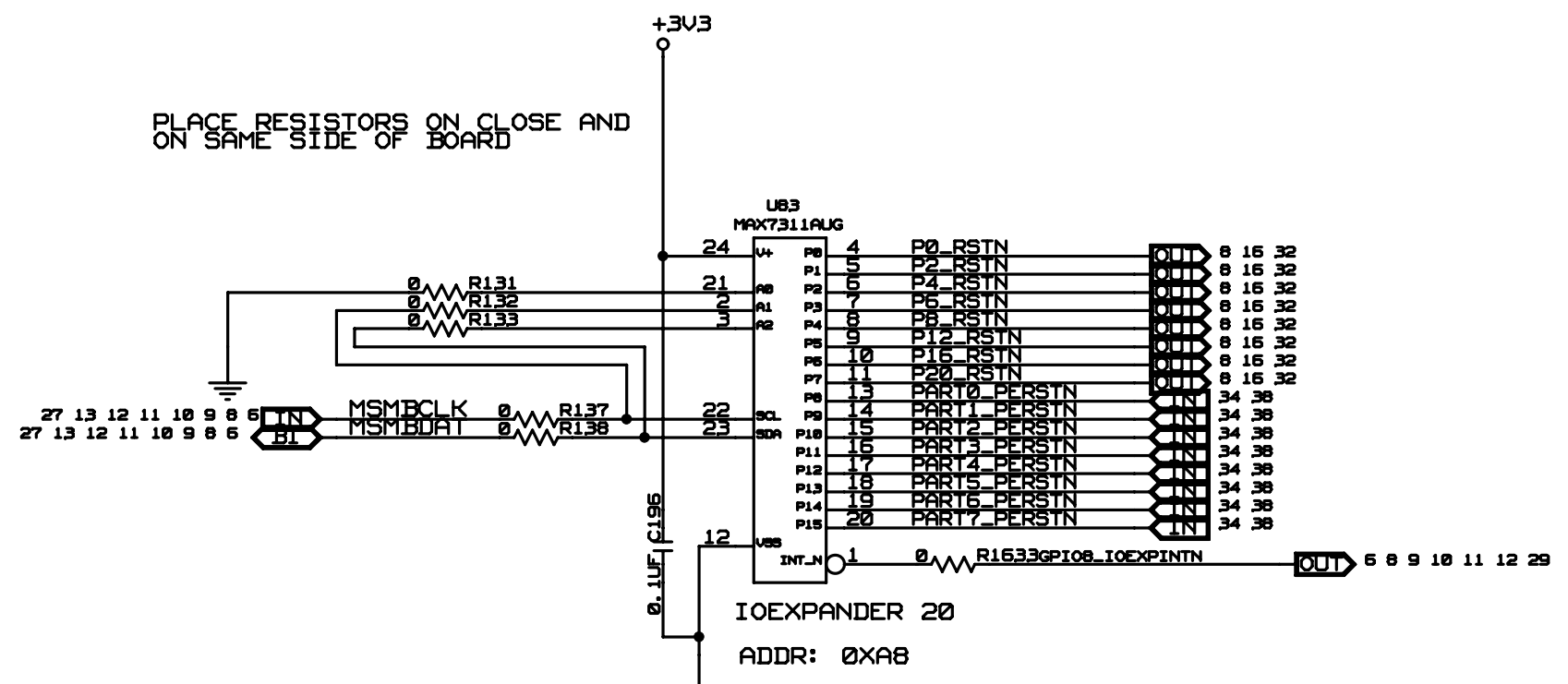
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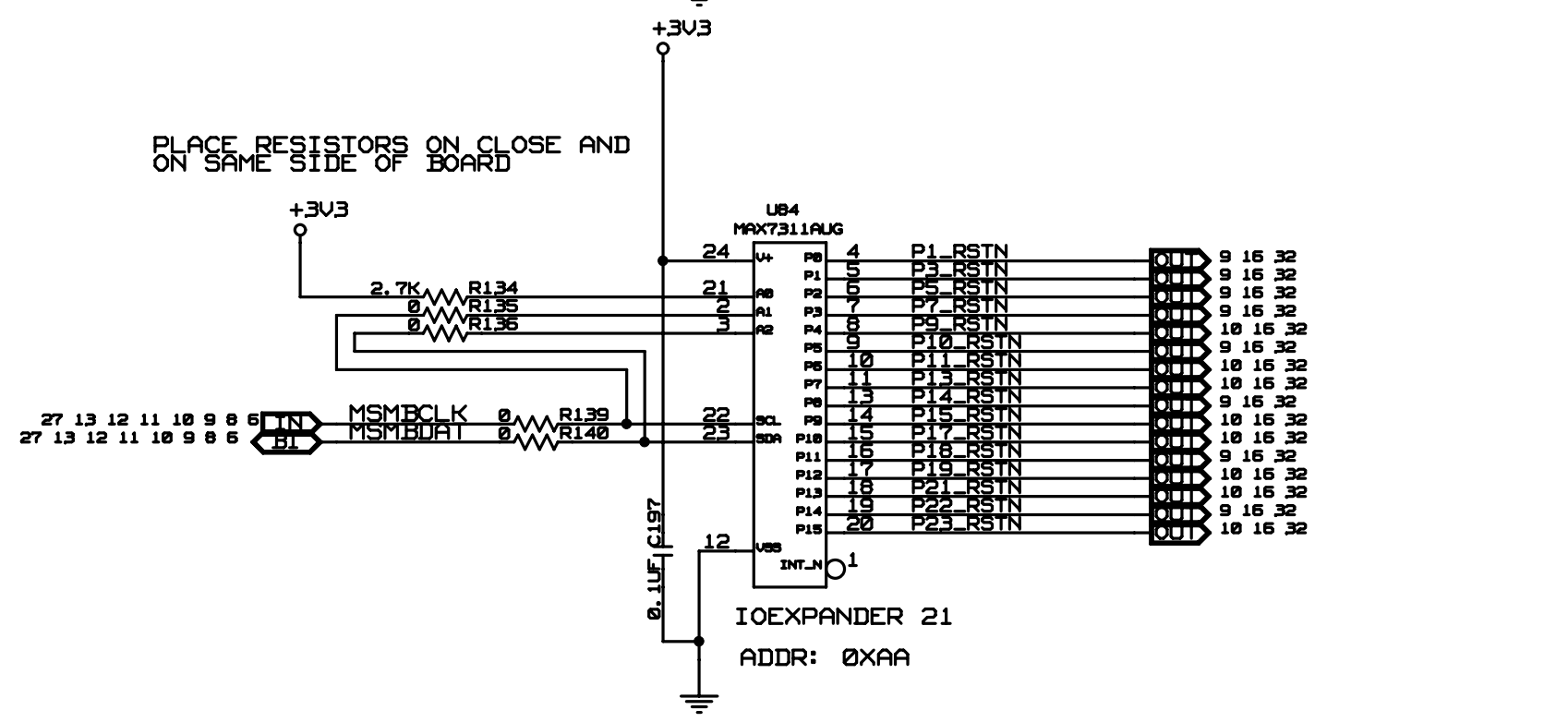
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| TITLE EB-LOGAN-19 | | | |
| IOEXPANDER 16-19 | | | |
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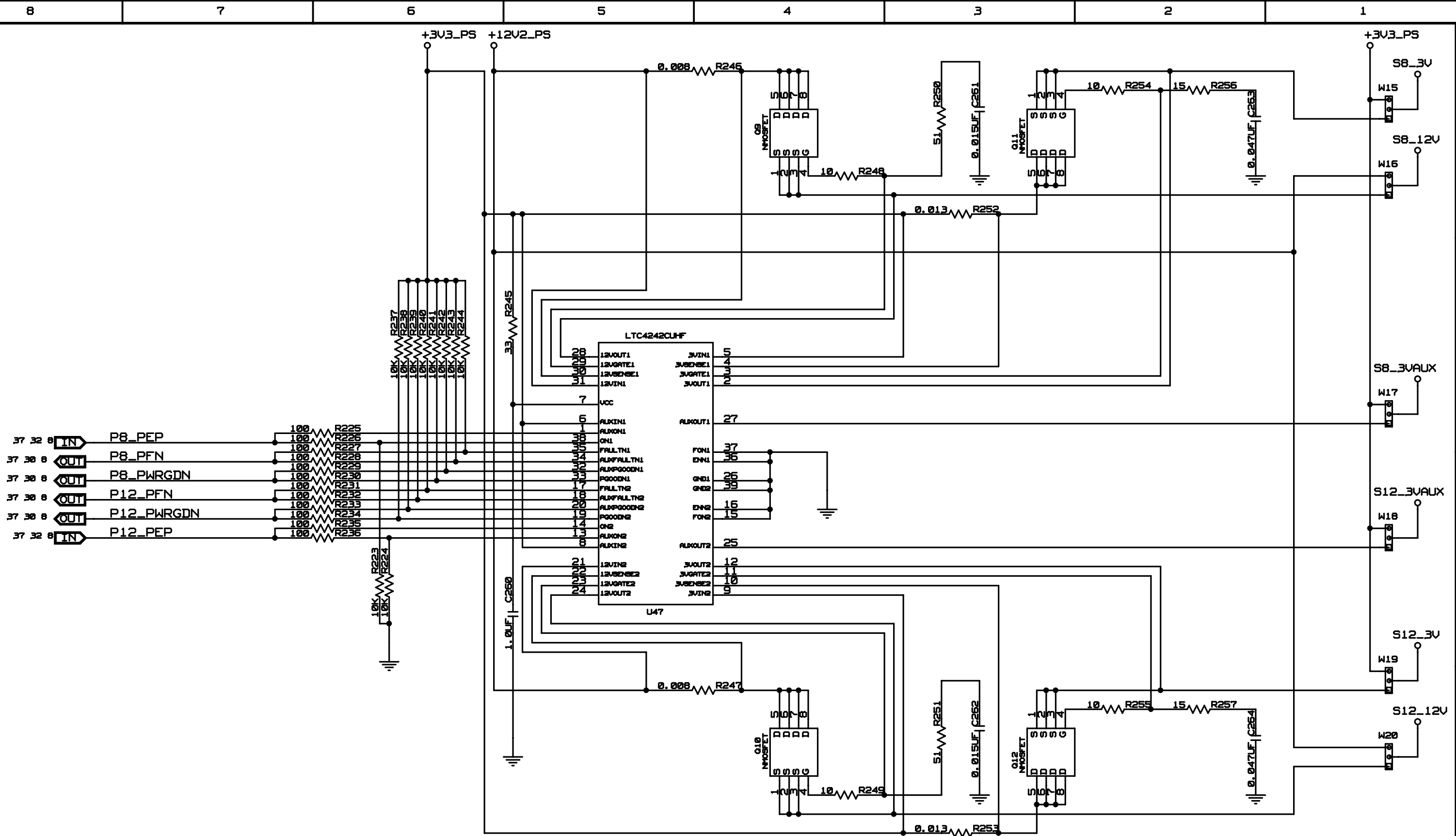


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| TITLE EB-LOGAN-19 | | | |
| IOEXPANDER 20-21 | | | |
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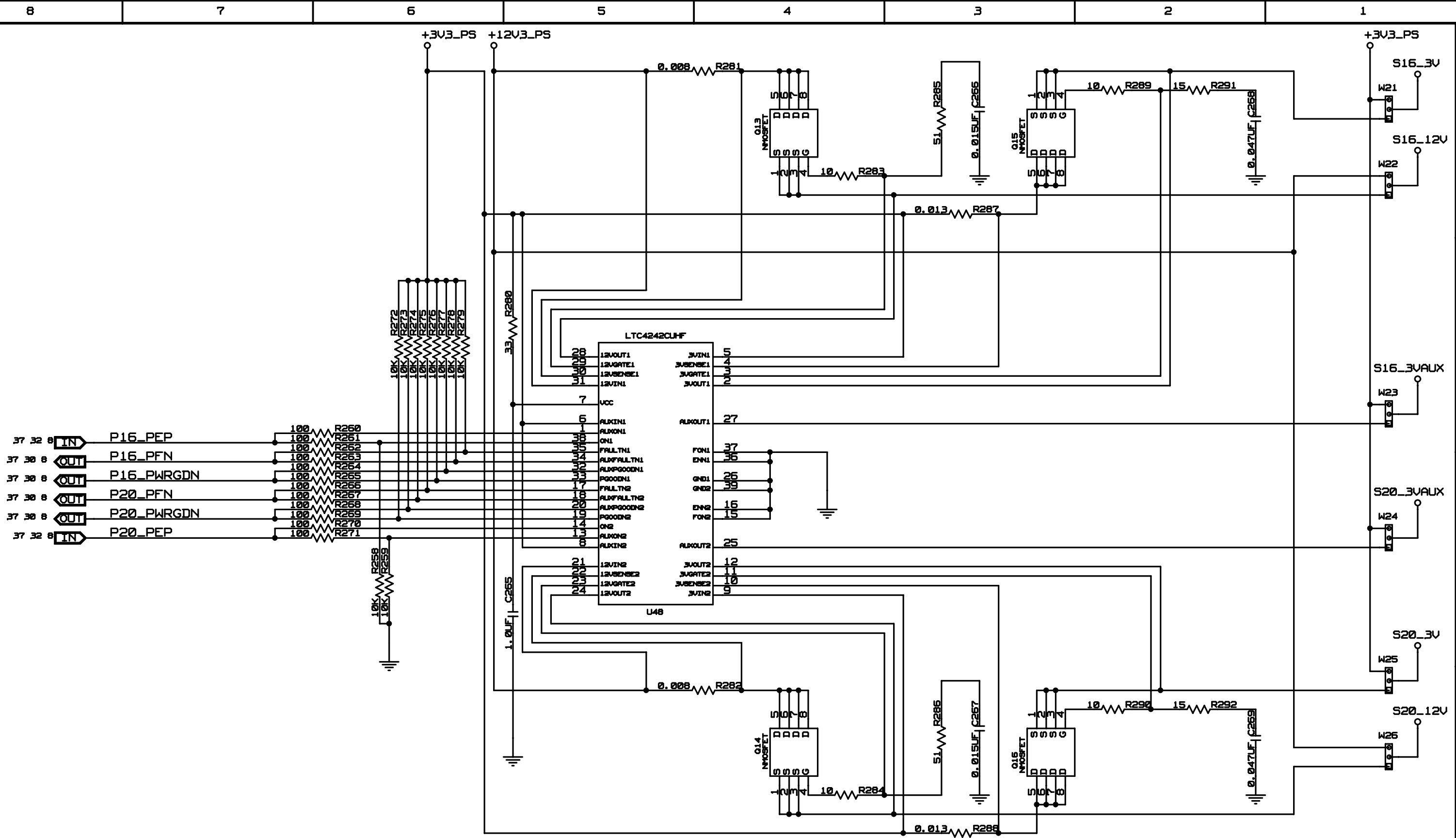
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HOT PLUG CONTROL PORTS 8-12

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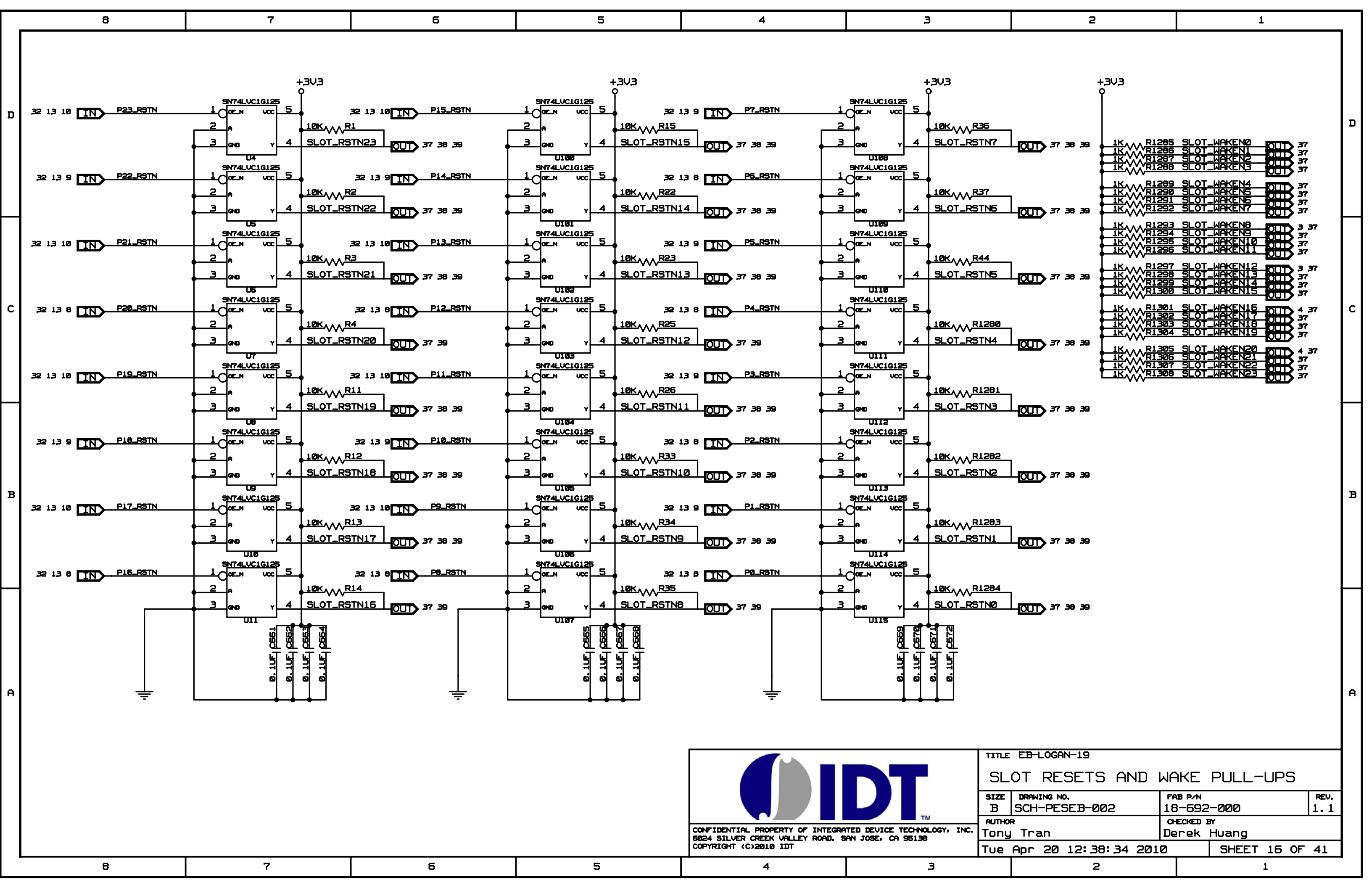
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| AUTHOR Tony Tran | CHECKED BY Derek Huang |
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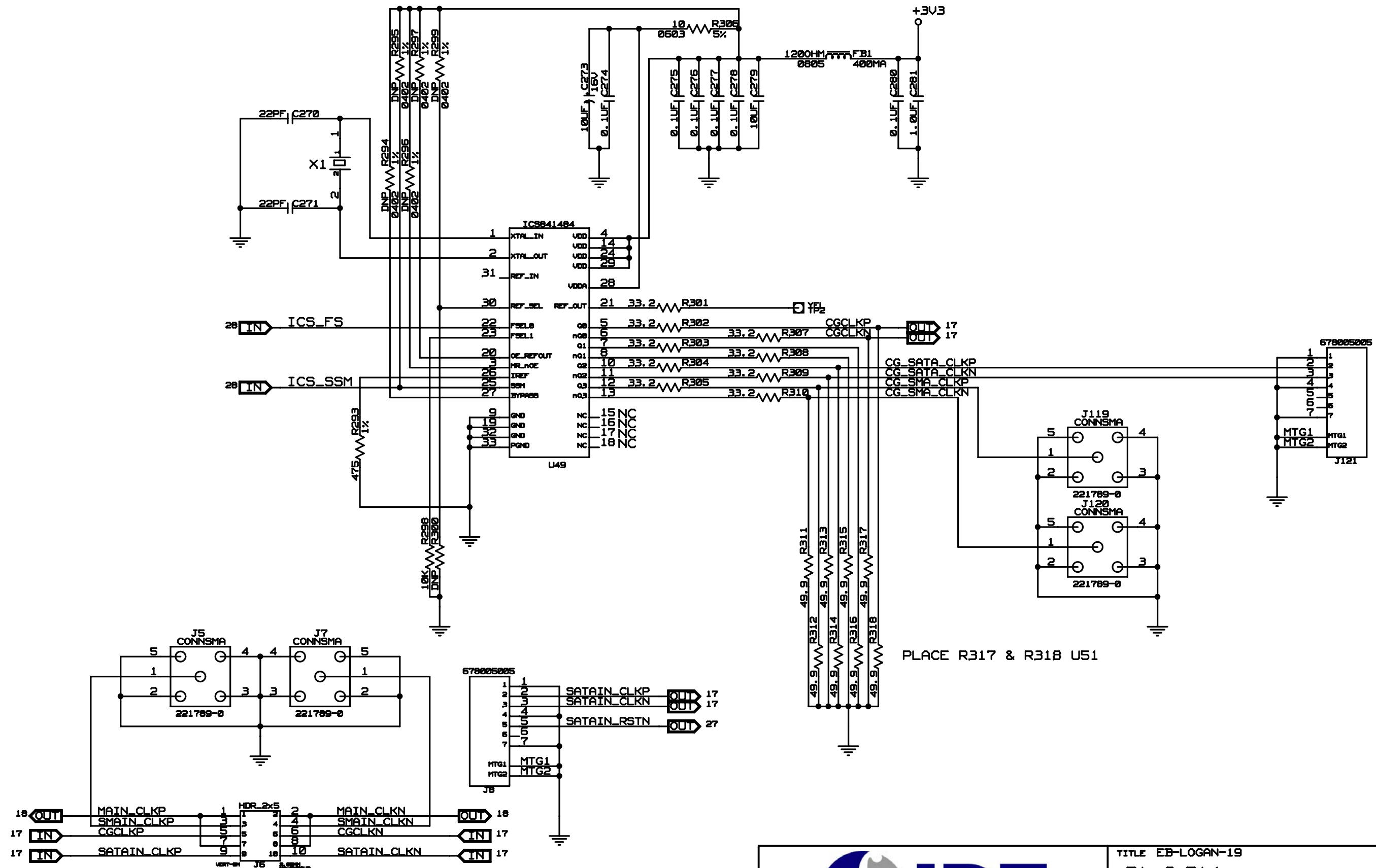
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| TITLE EB-LOGAN-19 | | | |
| HOT PLUG CONTROL PORTS 16-20 | | | |
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| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
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| TITLE EB-LOGAN-19 | | | |
| SLOT RESETS AND WAKE PULL-UPS | | | |
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PLACE R317 & R318 U51

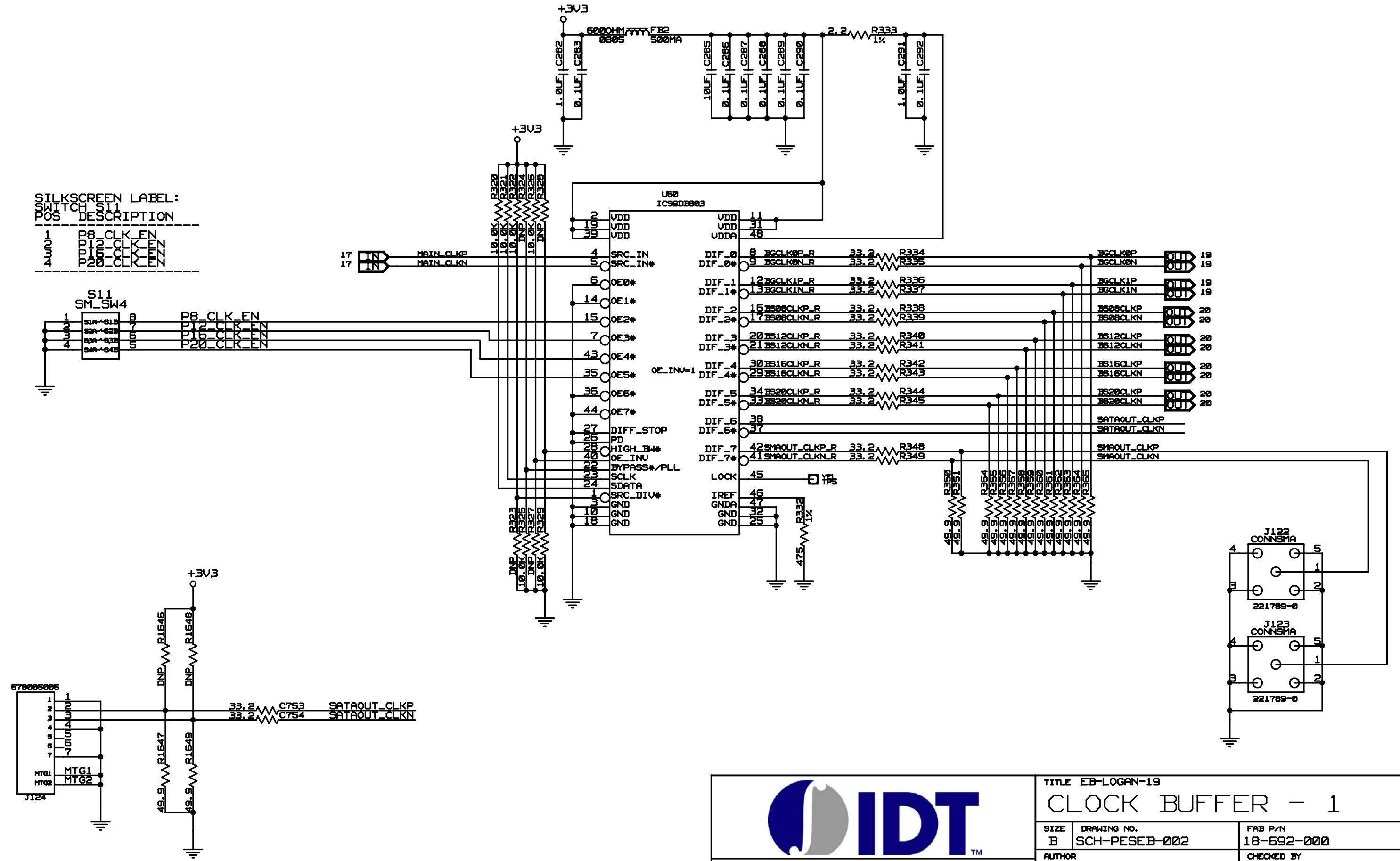
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| CLOCK | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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SILKSCREEN LABEL:
SWITCH S11

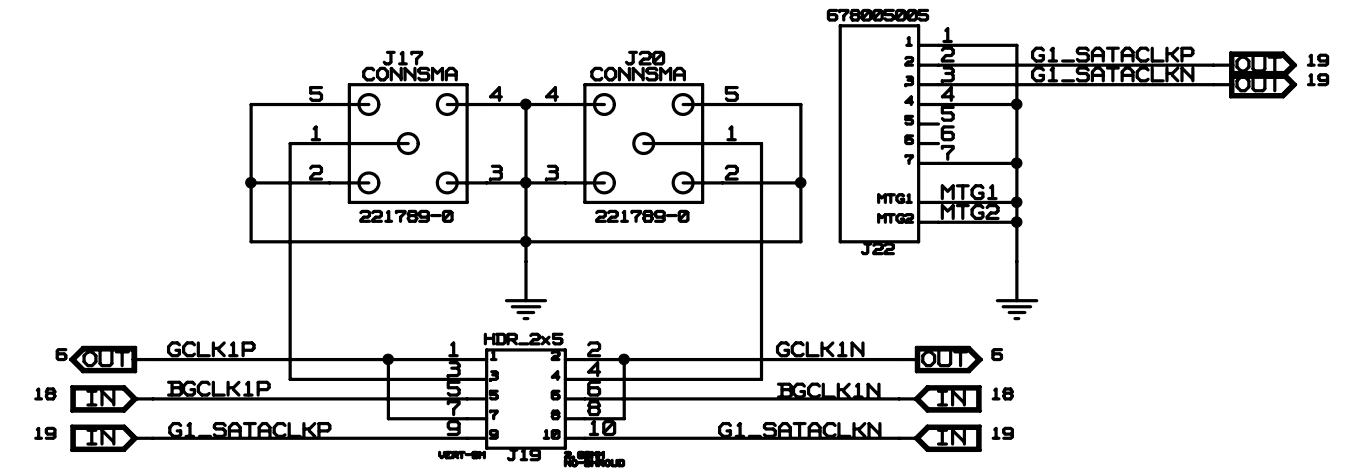
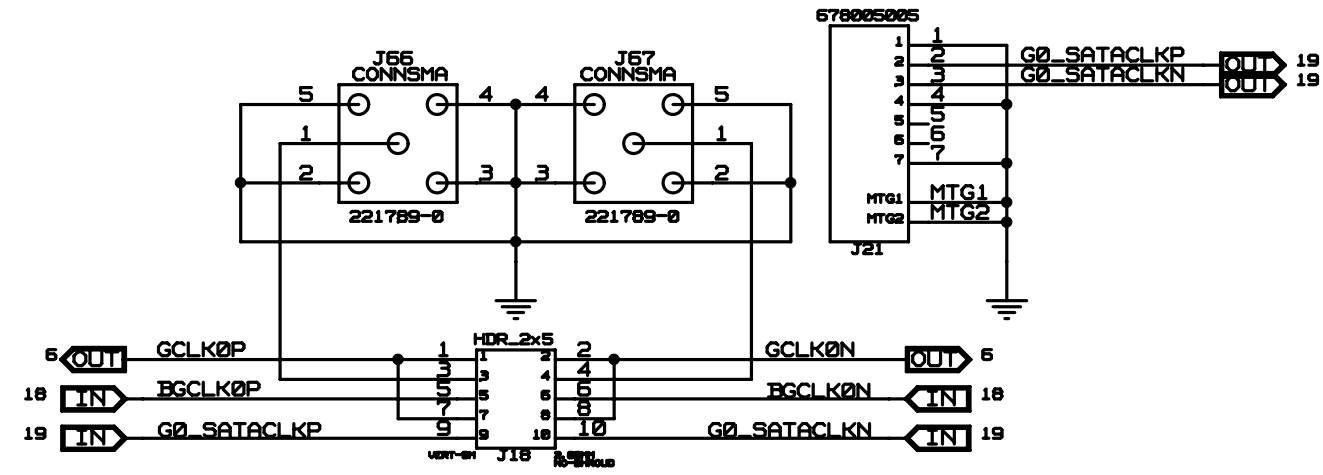
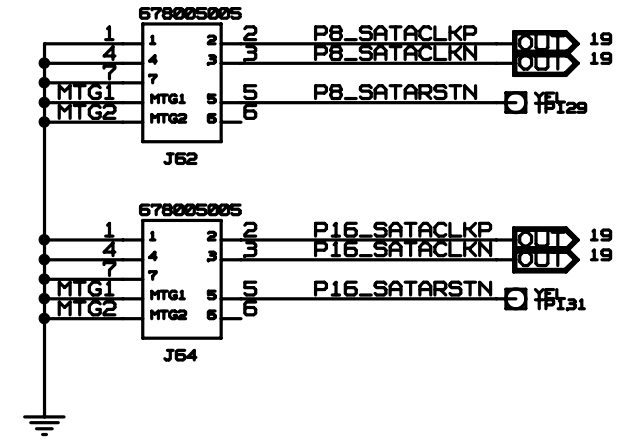
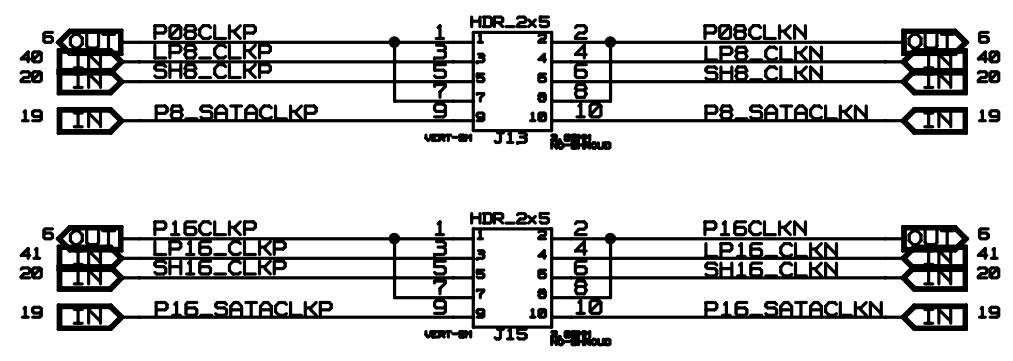
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| U11 | CLK |
| U20 | CLK |
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| YYY | EN |
| ZZZ | EN |



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|--------------------------|---------------|-------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| CLOCK BUFFER - 1 | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
| AUTHOR | | CHECKED BY | |
| Tony Tran | | Derek Huang | |
| Tue Apr 20 12:38:22 2010 | | | SHEET 18 OF 41 |

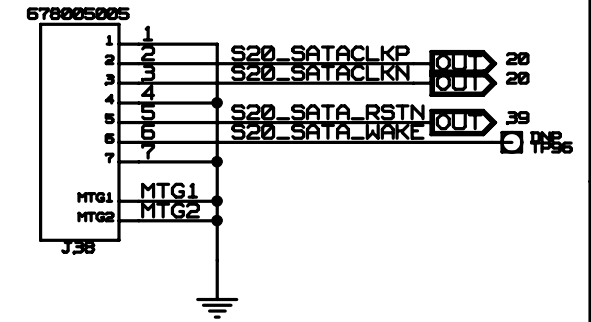
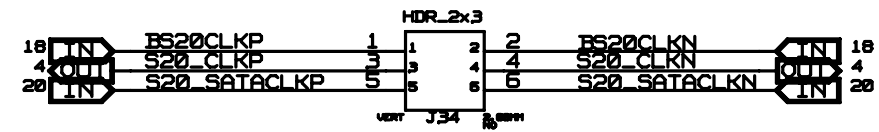
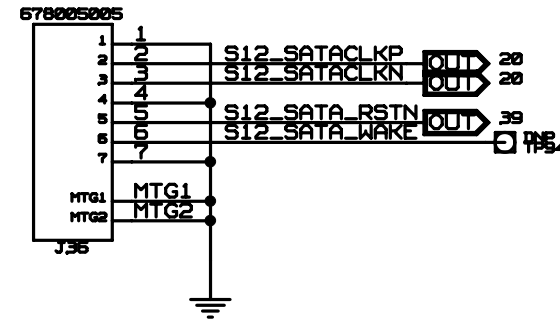
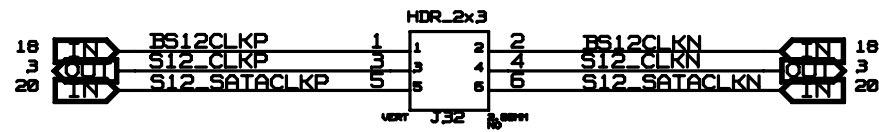
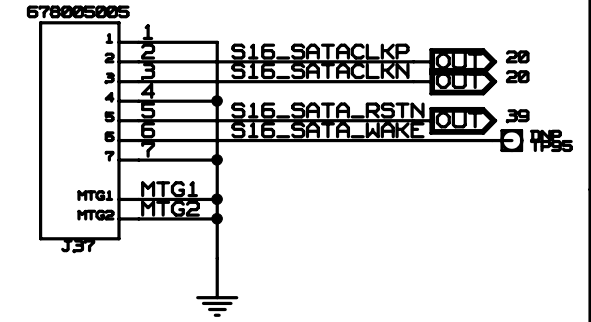
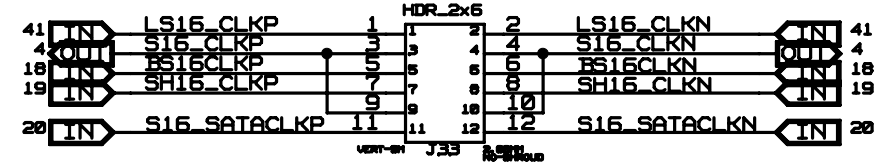
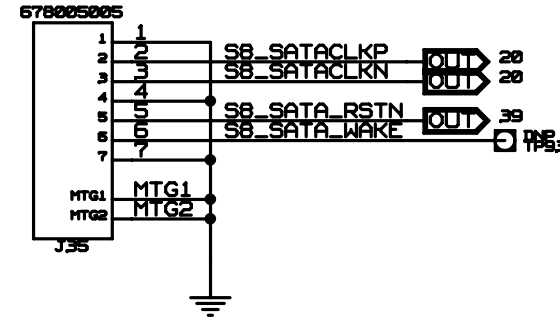
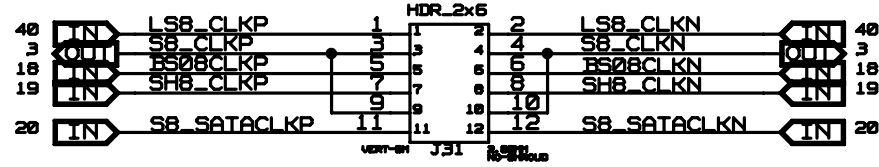
PXXCLK - DUT CLK
 LPXXCLK - LOCAL CLOCK GEN. PORT CLK
 SHXXCLK - SLOT HDR. CLK



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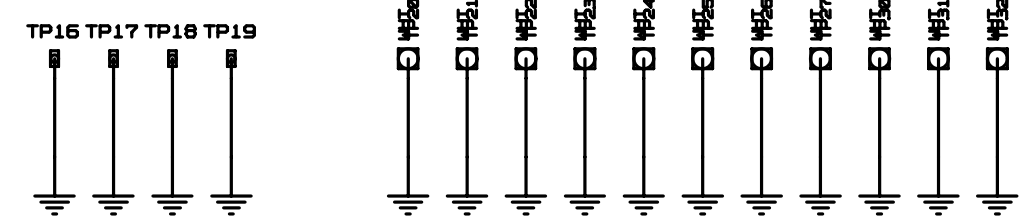
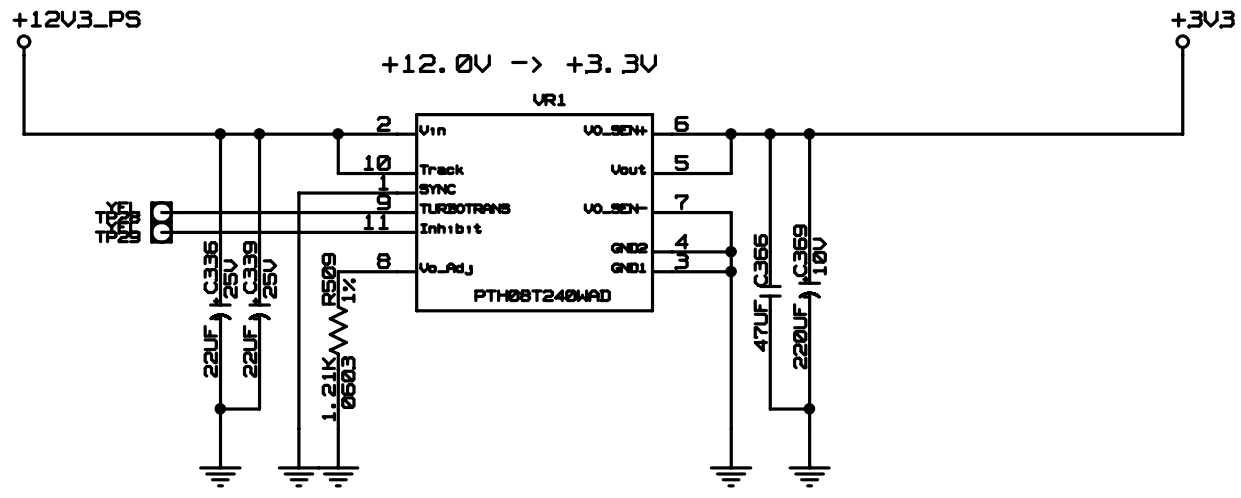
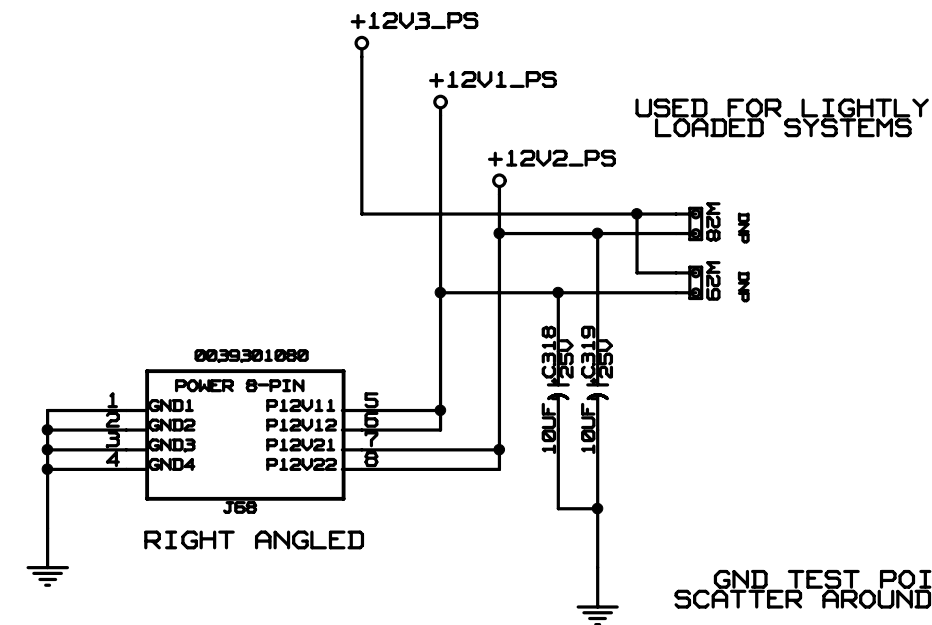
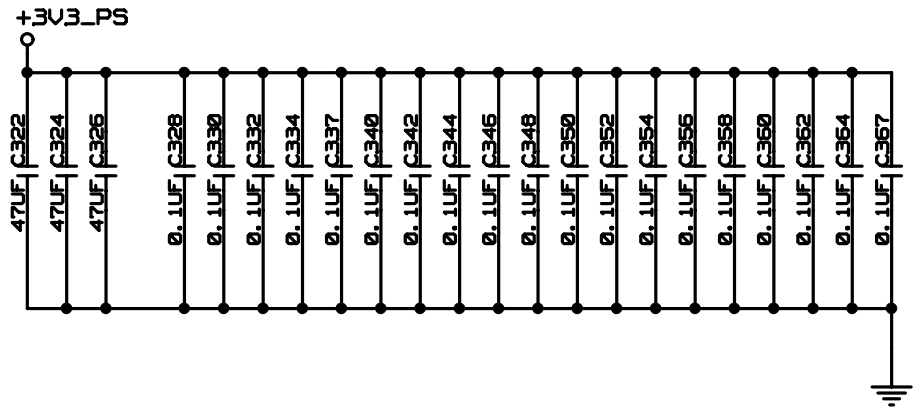
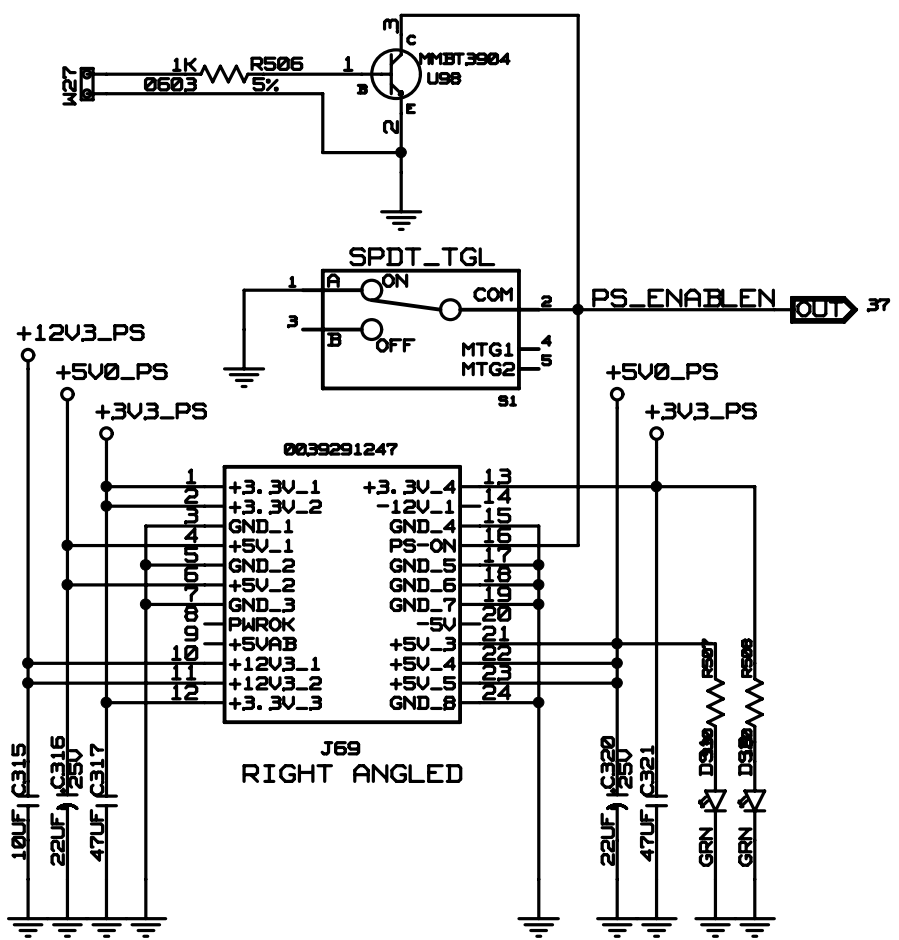
| | | | |
|--------------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| CLOCK SELECTOR DUT PCLK 8 & 16 | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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SXCLK - SLOT CLK
 BSXCLK - BUFFER SLOT CLK
 LSXCLK - LOCAL CLOCK GEN. SLOT CLK
 SHXCLK - SLOT HDR. CLK



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| | | | |
|---------------------------|---------------|-------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| CLOCK SELECTOR SLOTS 8-20 | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
| AUTHOR | | CHECKED BY | |
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| | | | |
|--------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| POWER CONNECTORS | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:22 2010 | | | SHEET 21 OF 41 |

D

C

B

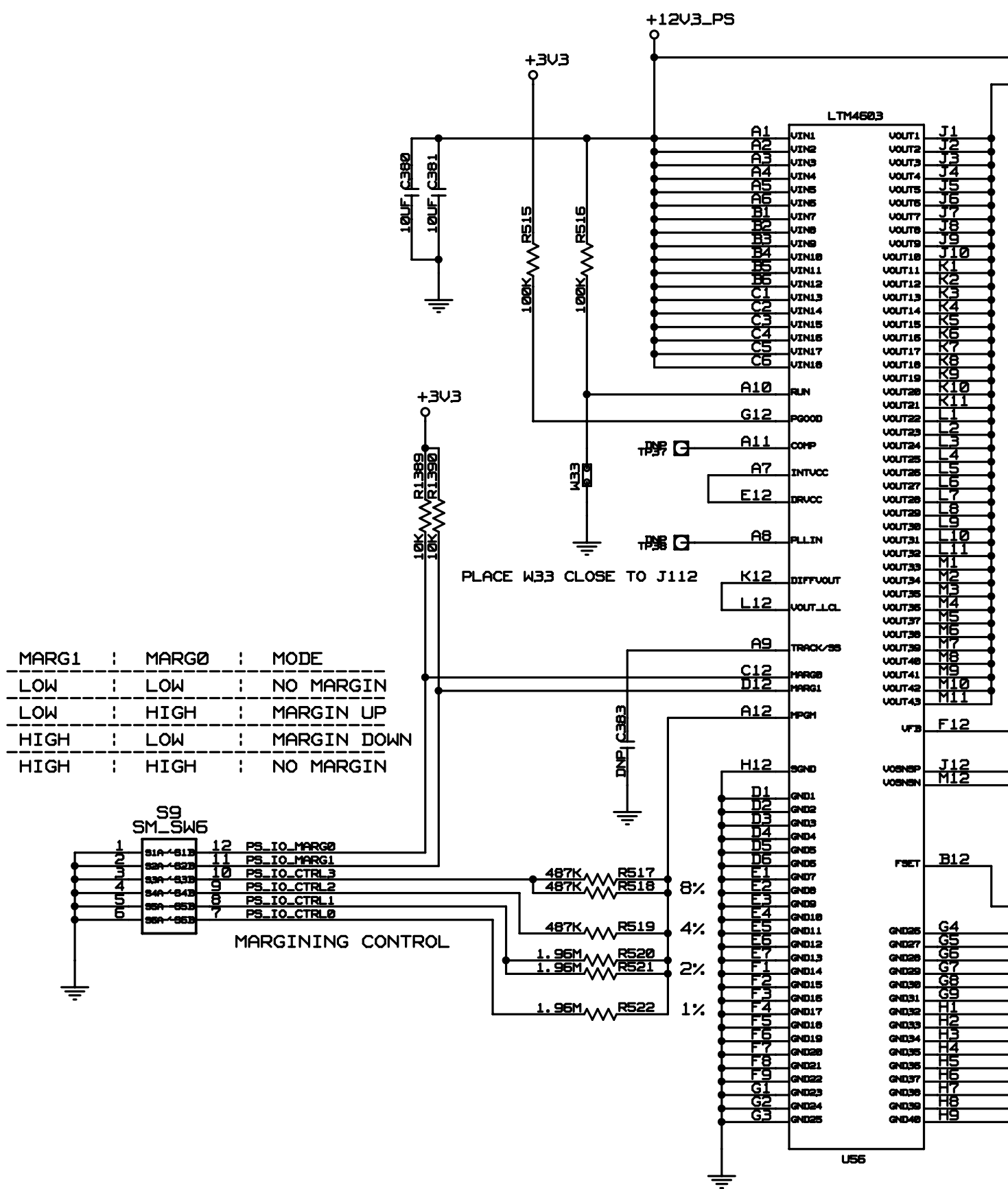
A

D

C

B

A



| MARG1 | MARG0 | MODE |
|-------|-------|-------------|
| LOW | LOW | NO MARGIN |
| LOW | HIGH | MARGIN UP |
| HIGH | LOW | MARGIN DOWN |
| HIGH | HIGH | NO MARGIN |

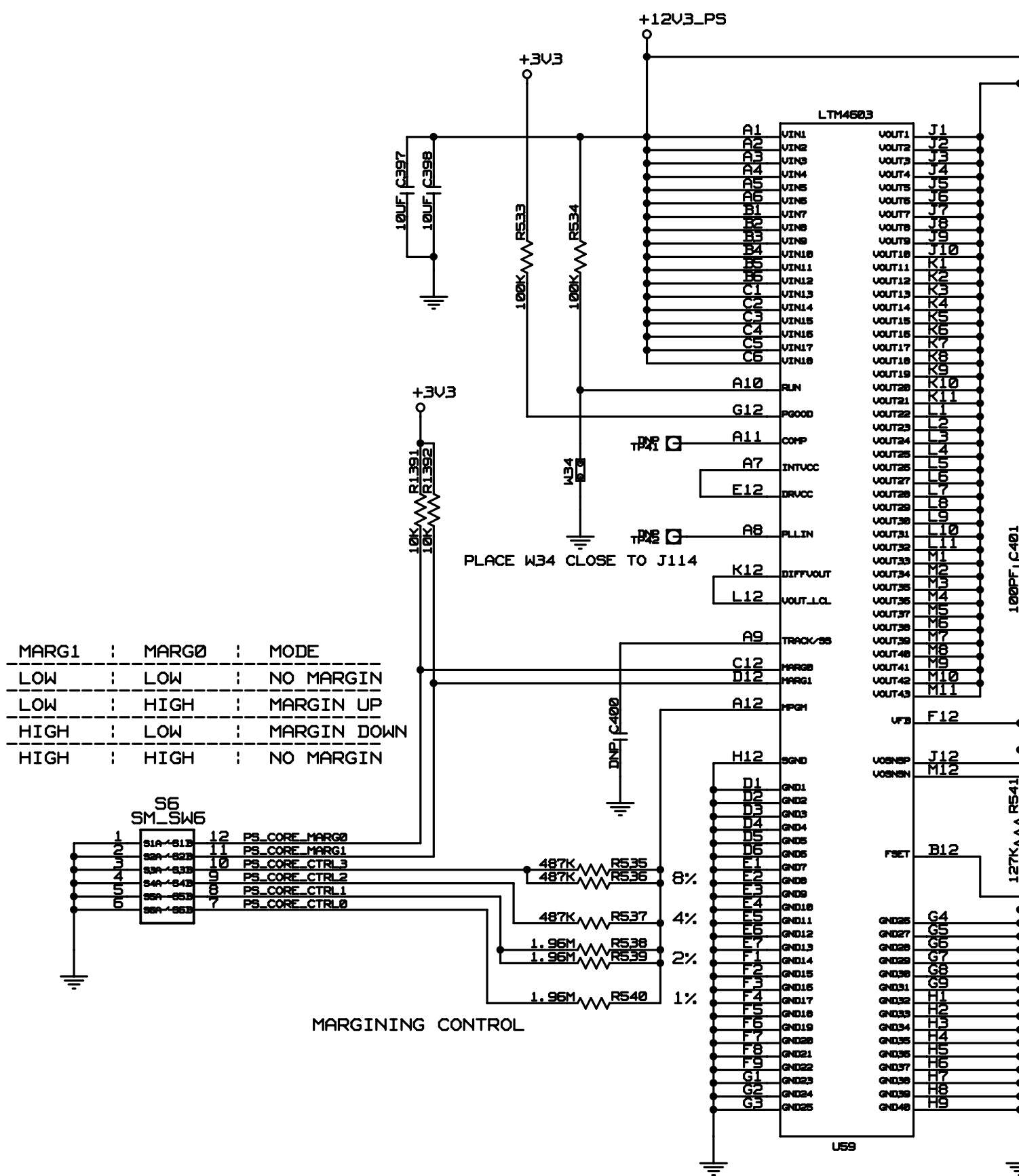
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| | | | |
|--------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| POWER REGULATOR - VDDIO | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:23 2010 | | | SHEET 22 OF 41 |

ROUTE AS POWER NET OR ISLAND
 REG_2V5_VDDIO

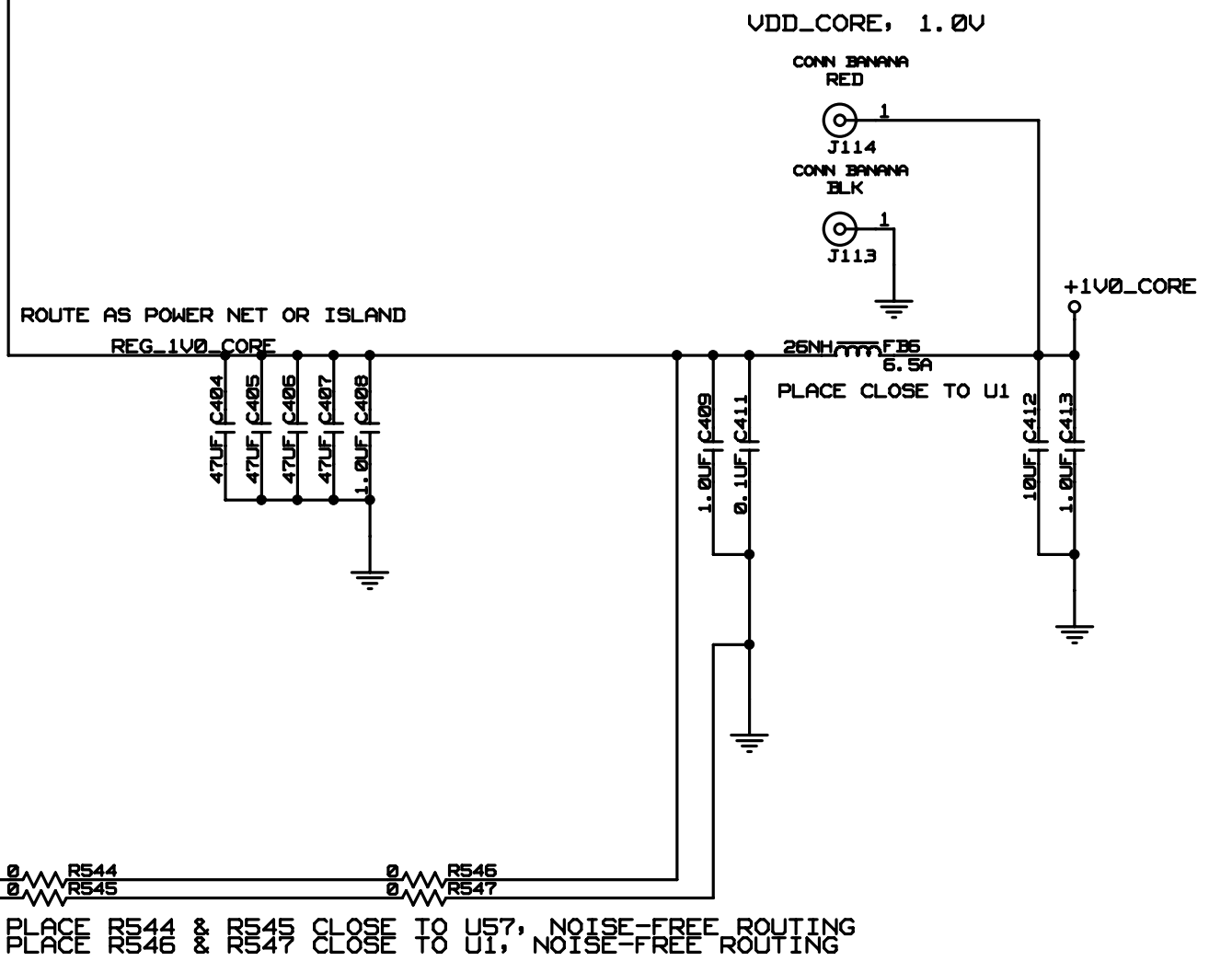
VDD_IO, 3.3V
 CONN BANANA RED
 CONN BANANA BLK

PLACE R526 & R527 CLOSE TO U57, NOISE-FREE ROUTING
 PLACE R528 & R529 CLOSE TO U1, NOISE-FREE ROUTING



| MARG1 | MARG0 | MODE |
|-------|-------|-------------|
| LOW | LOW | NO MARGIN |
| LOW | HIGH | MARGIN UP |
| HIGH | LOW | MARGIN DOWN |
| HIGH | HIGH | NO MARGIN |

MARGINING CONTROL

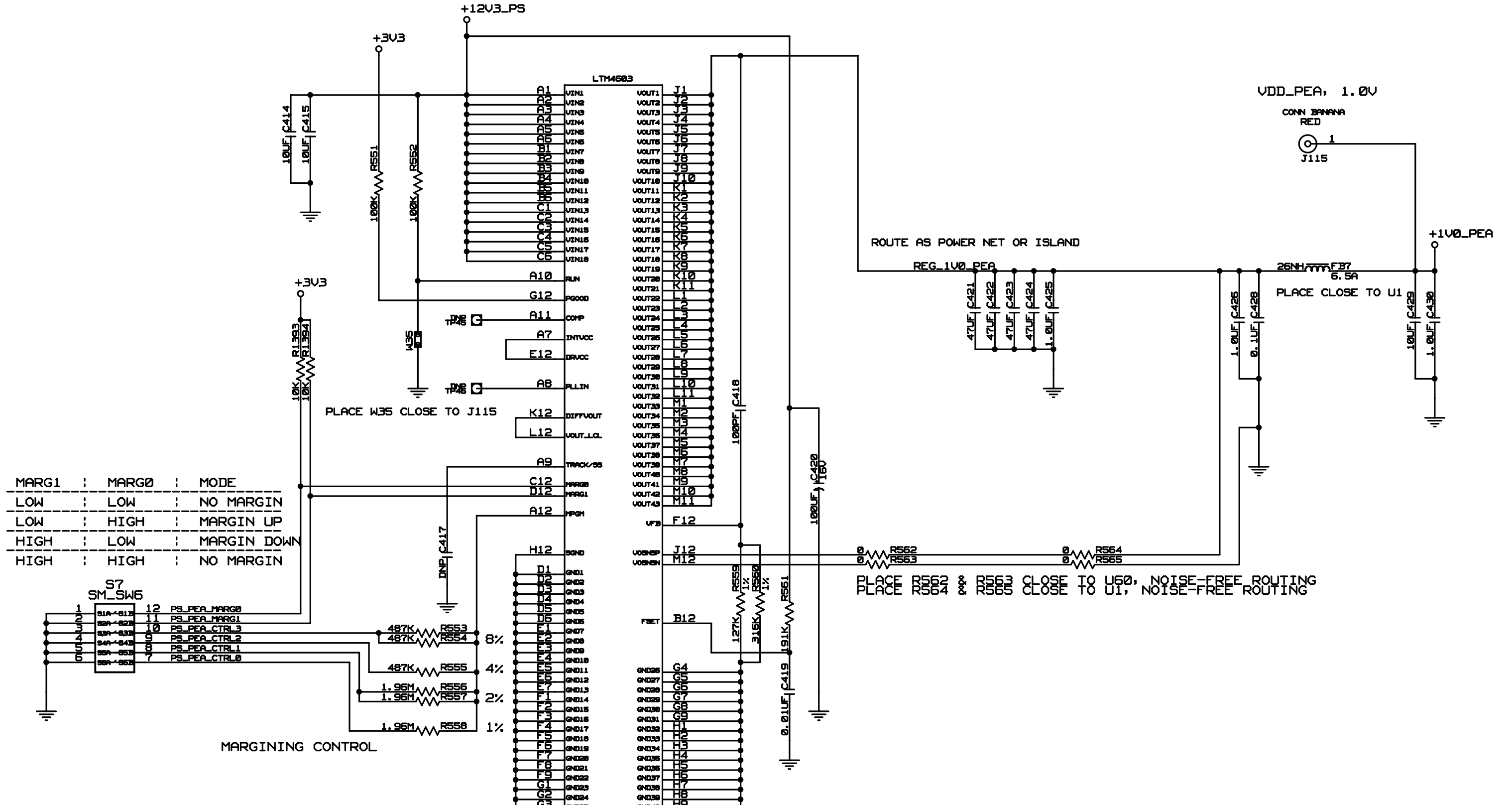


PLACE R544, R545 CLOSE TO U57, NOISE-FREE ROUTING
 PLACE R546, R547 CLOSE TO U1, NOISE-FREE ROUTING



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| | | | |
|---------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| POWER REGULATOR - VDDCORE | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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| | | | |
|--------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| POWER REGULATOR - VDDPEA | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:24 2010 | | | SHEET 24 OF 41 |

D

C

B

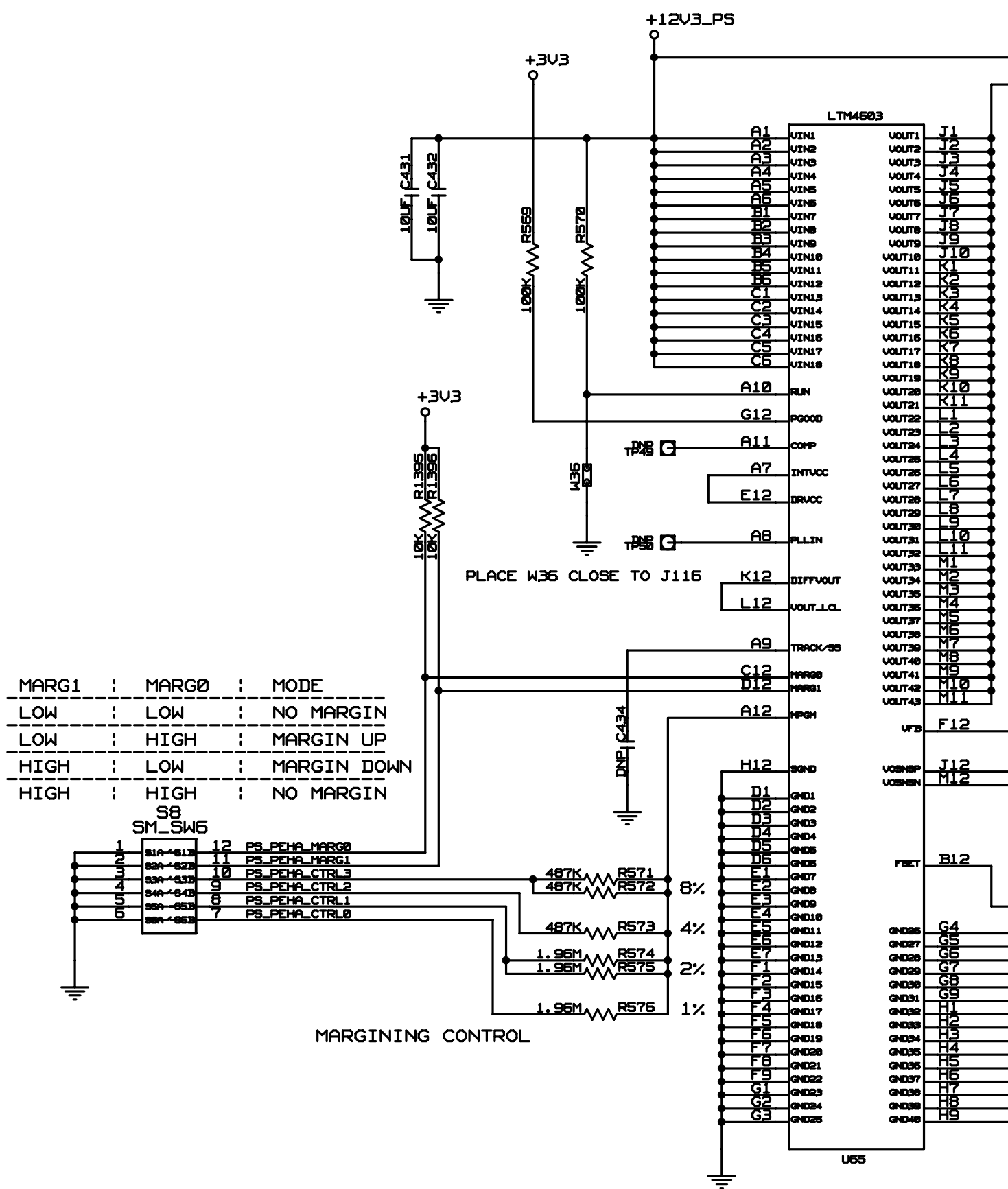
A

D

C

B

A



| MARG1 | MARG0 | MODE |
|-------|-------|-------------|
| LOW | LOW | NO MARGIN |
| LOW | HIGH | MARGIN UP |
| HIGH | LOW | MARGIN DOWN |
| HIGH | HIGH | NO MARGIN |

MARGINING CONTROL

ROUTE AS POWER NET OR ISLAND
REG_2V5_PEHA

VDD_PEHA, 2.5V

CONN BANANA RED

J116

+2V5_PEHA

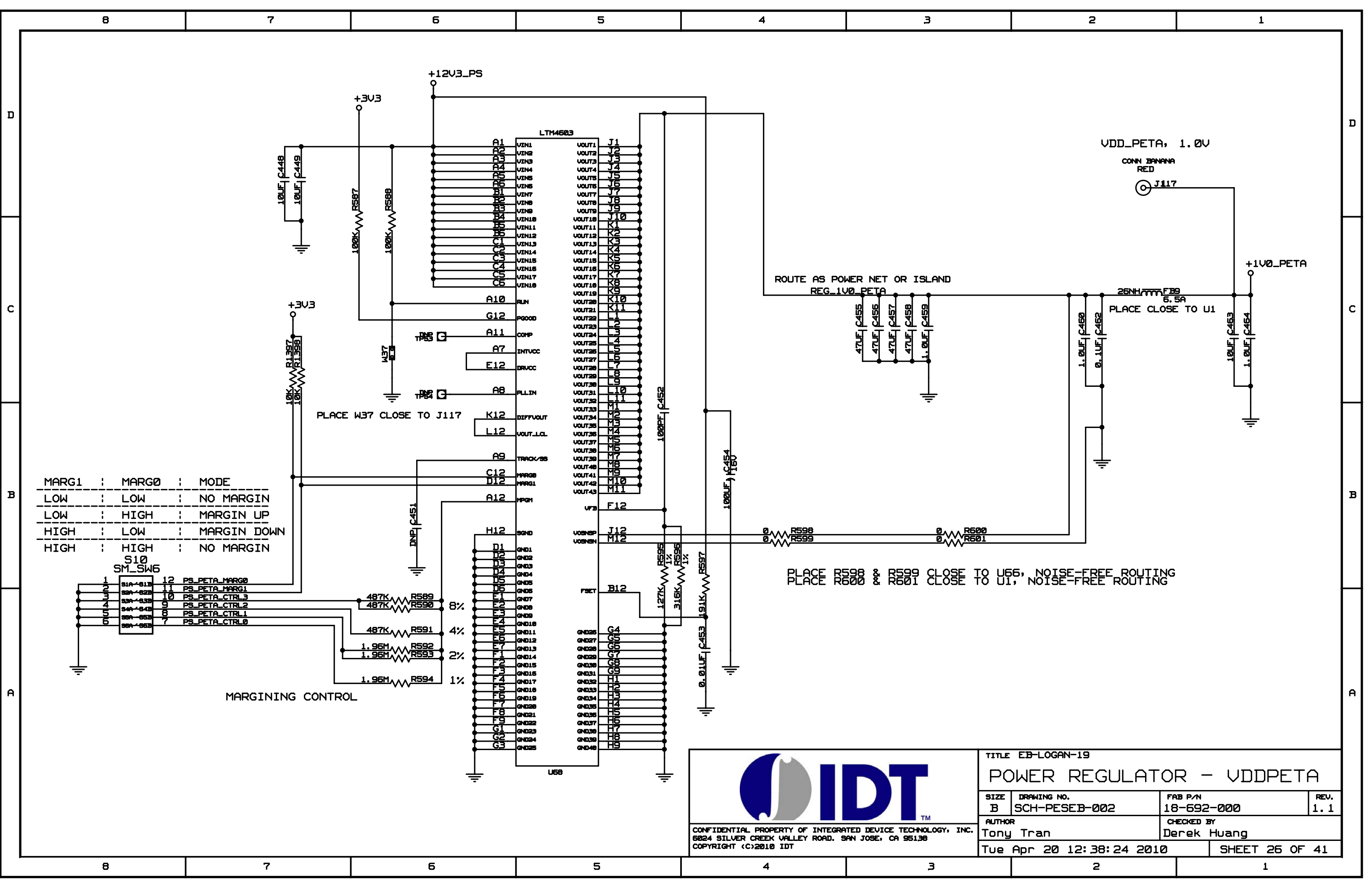
26NHz FB6
6.5A
PLACE CLOSE TO U1

PLACE R580, R581 CLOSE TO U53, NOISE-FREE ROUTING
PLACE R582, R583 CLOSE TO U1, NOISE-FREE ROUTING

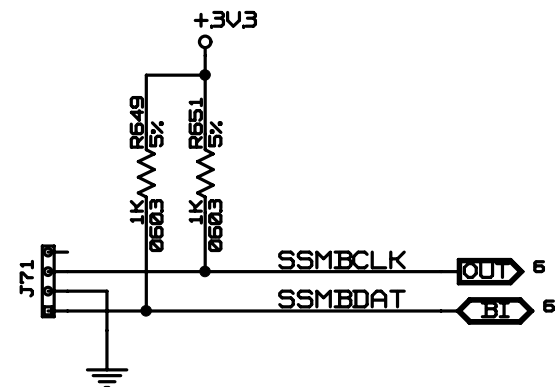
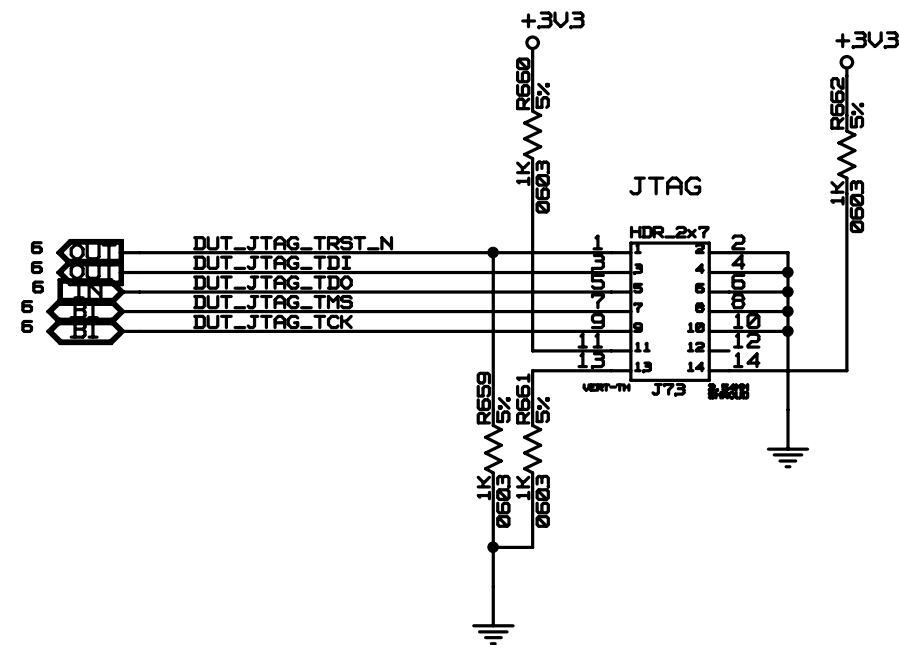
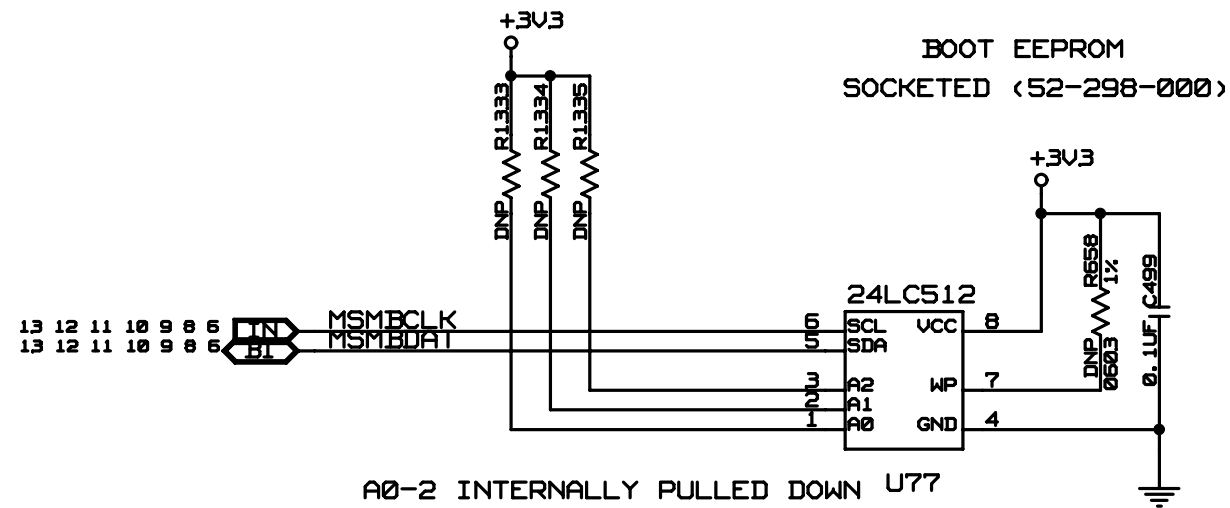
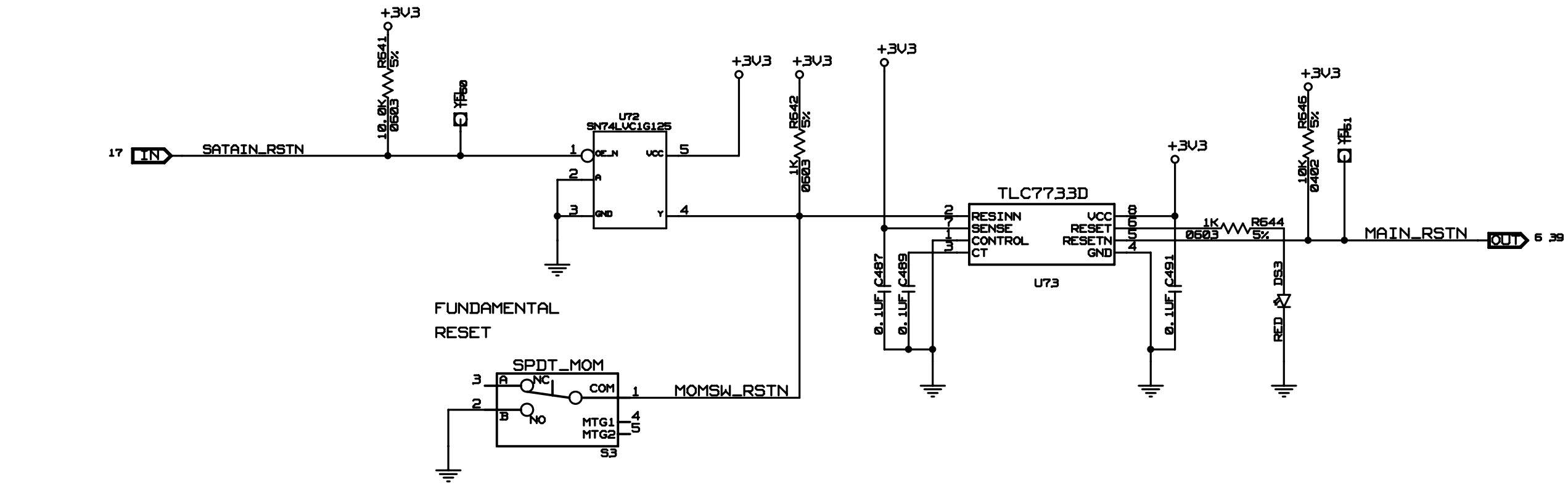


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| | | | |
|---------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| POWER REGULATOR - VDDPEHA | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:24 2010 | | | SHEET 25 OF 41 |

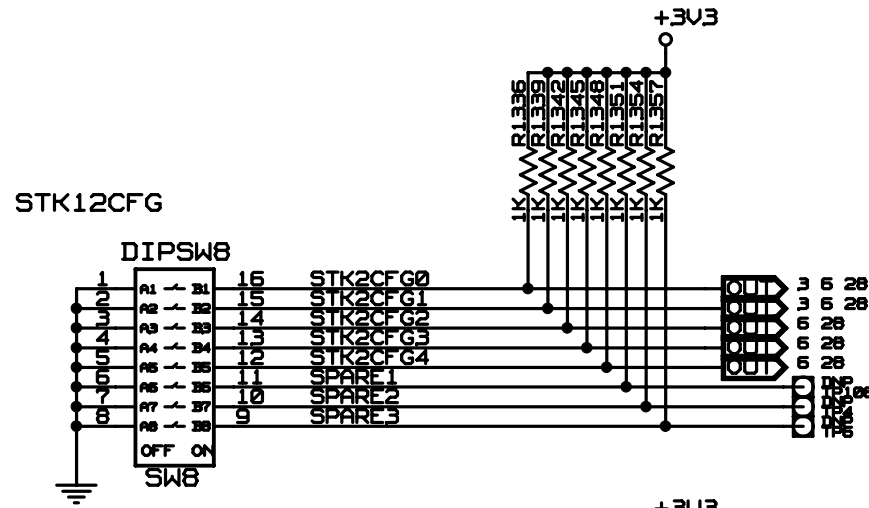


| | | | |
|---------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| POWER REGULATOR - VDDPETA | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:24 2010 | | | SHEET 26 OF 41 |

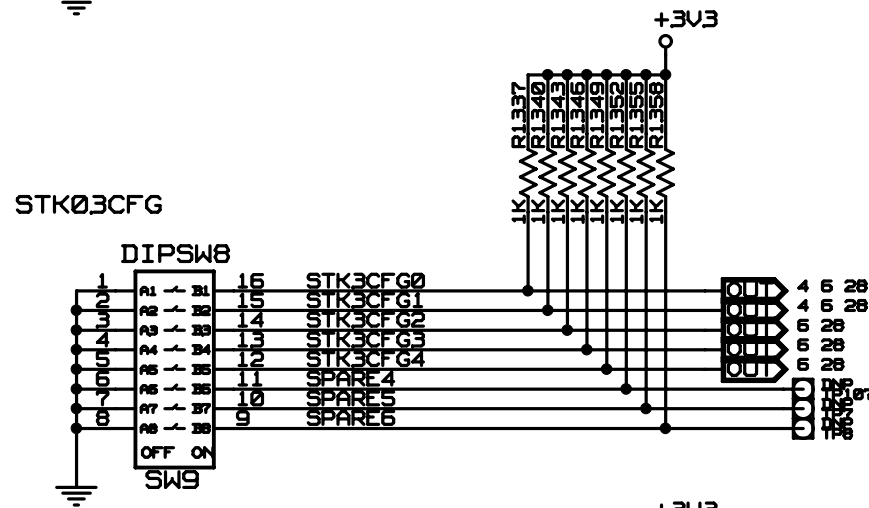
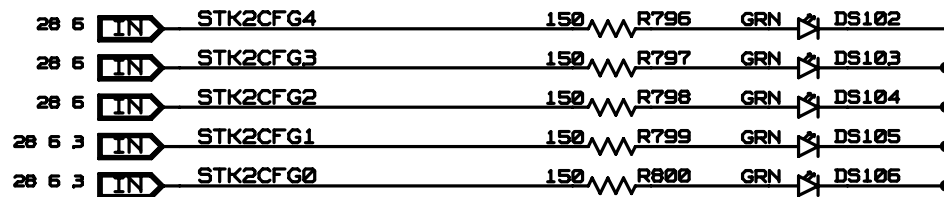


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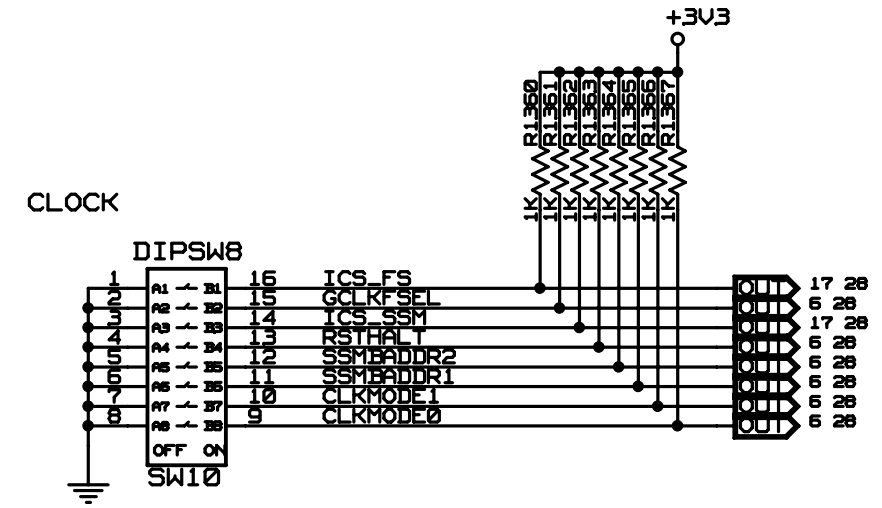
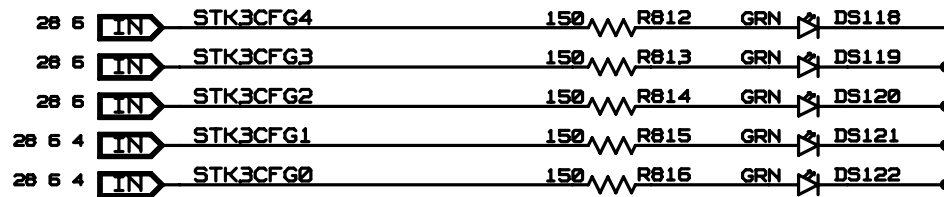
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|----------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| RESET, SMBUS, EEPROM, JTAG | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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<GREEN> ACTIVE HIGH - DIP STK12CFG

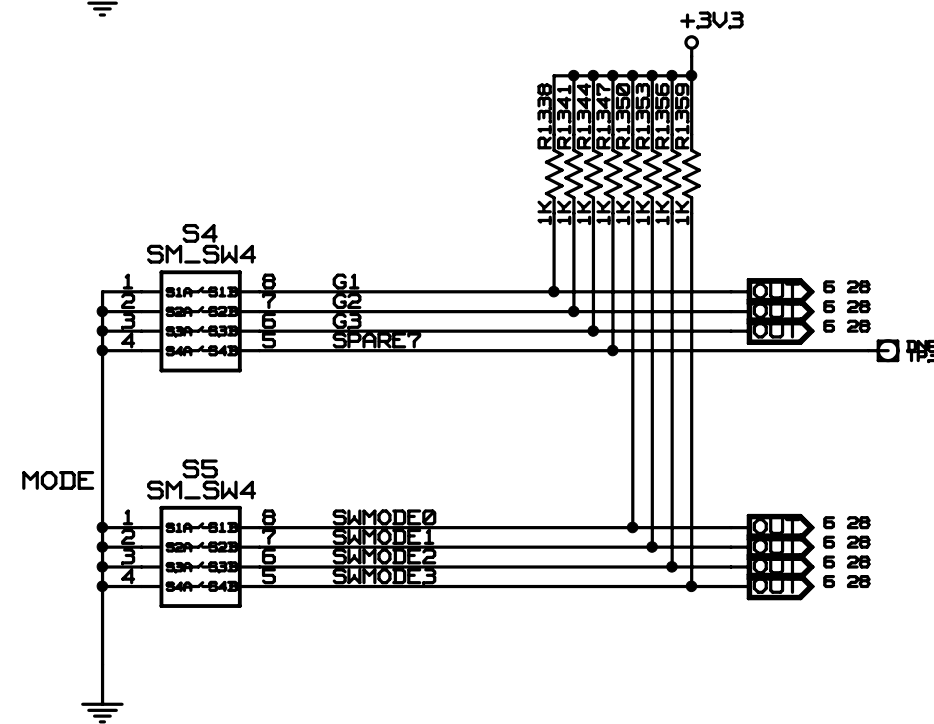
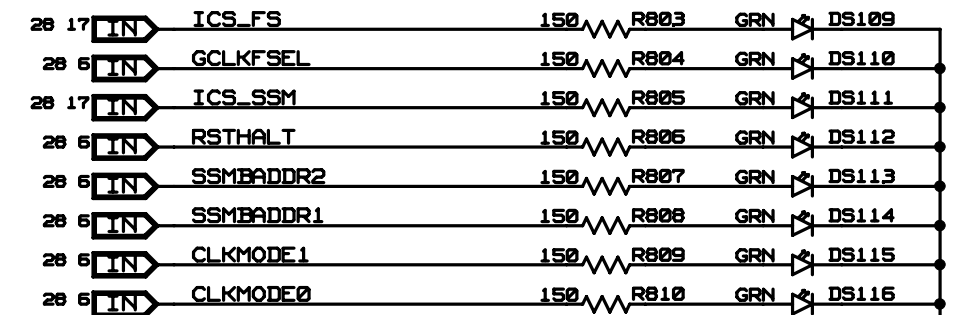


<GREEN> ACTIVE HIGH - DIP STK03CFG

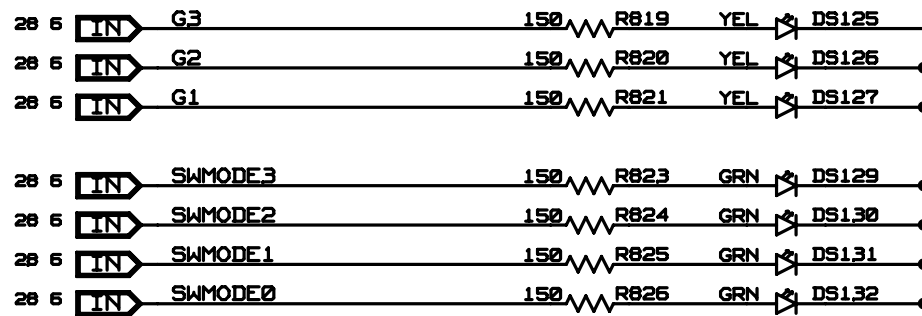


CLOCK

<GREEN> ACTIVE HIGH - DIP CLOCK

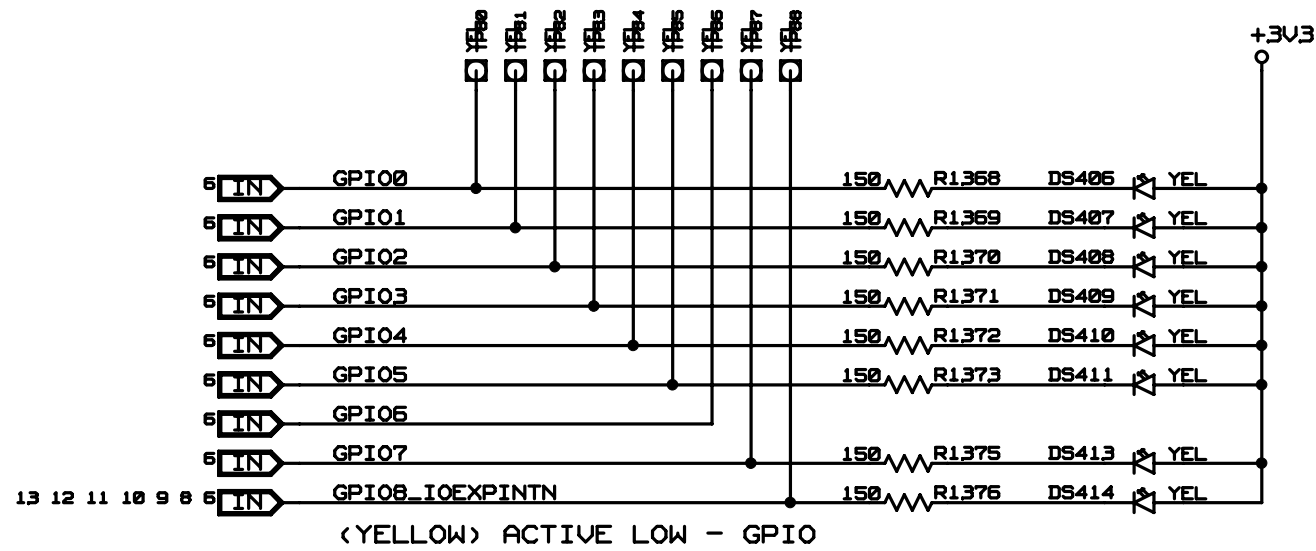


<GREEN> ACTIVE HIGH - DIP MODE

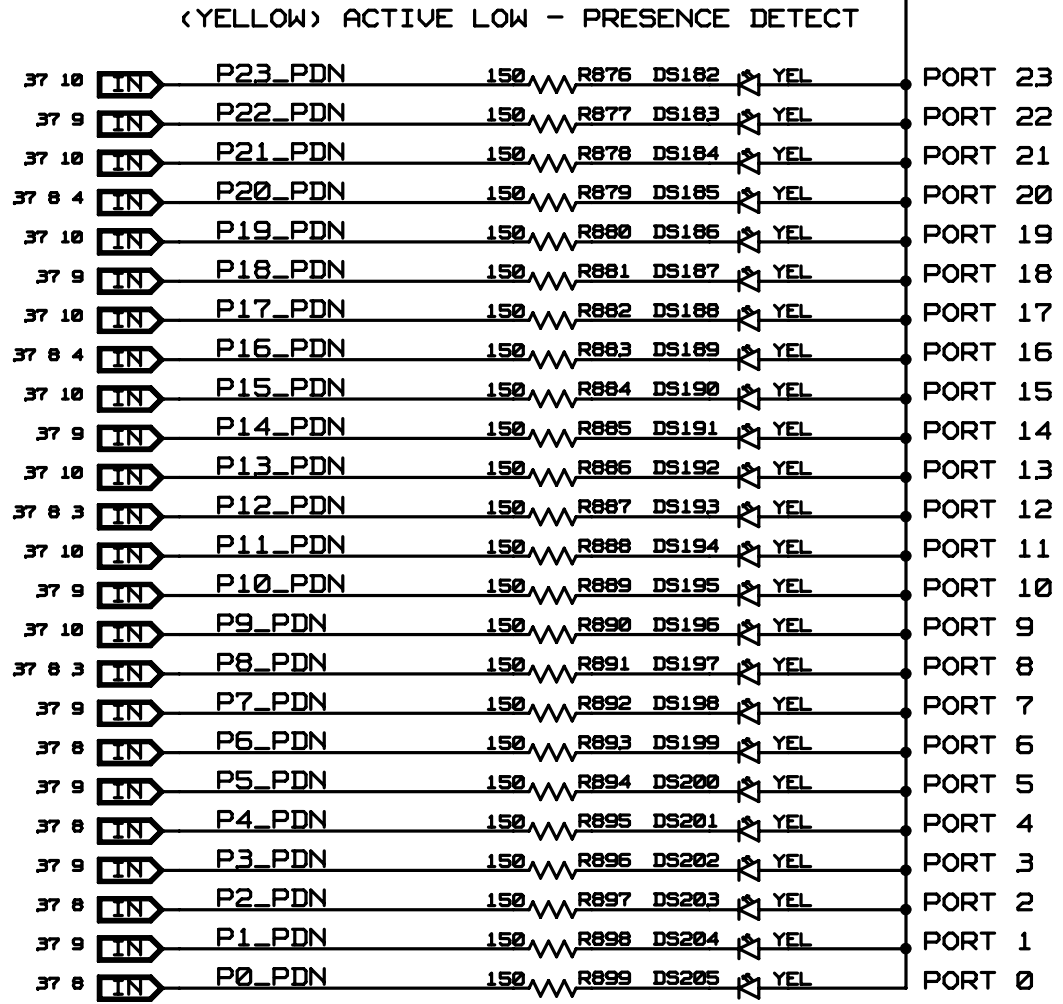
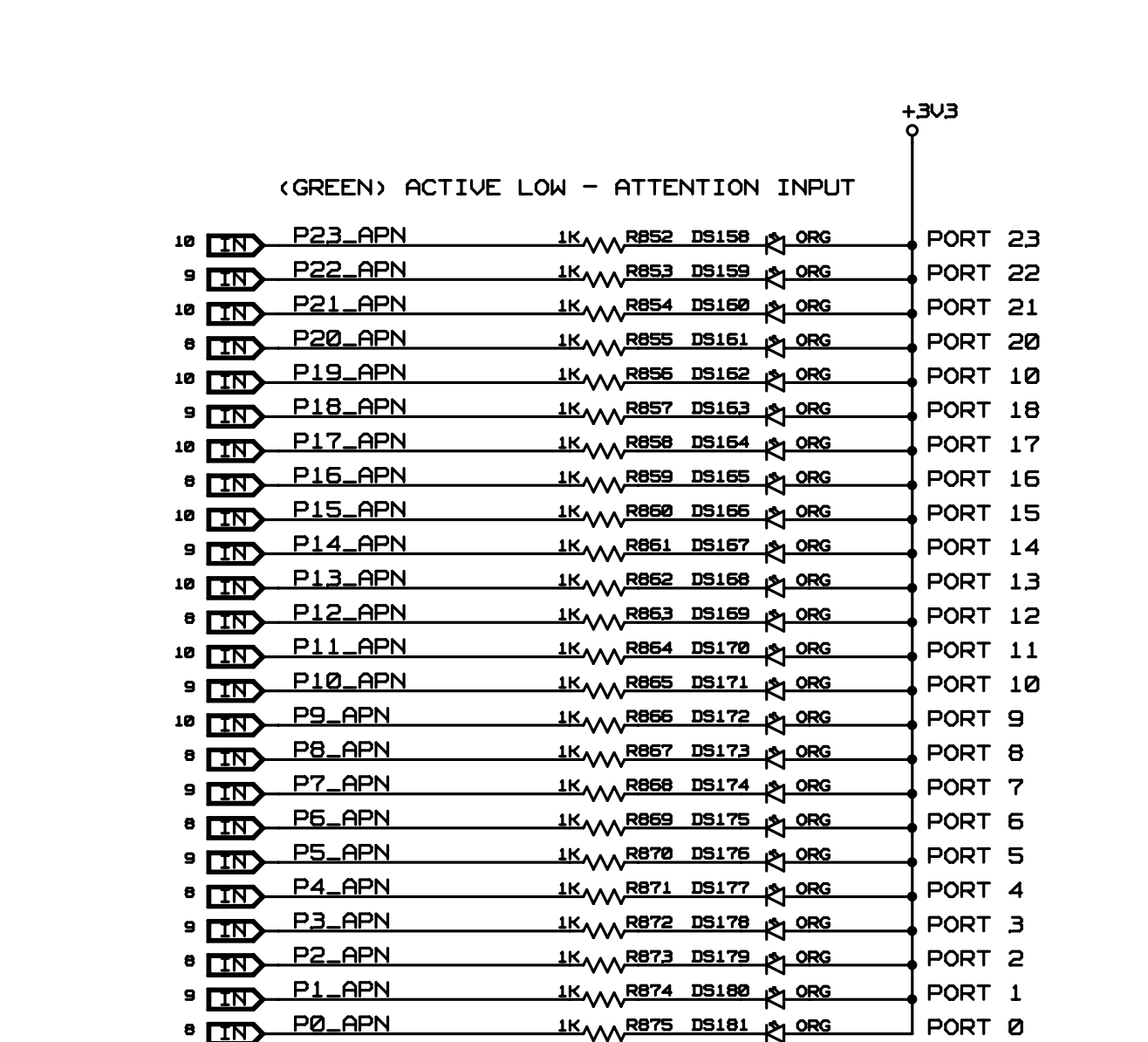


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| | | | |
|--------------------------|---------------|-------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| DIP SWITCHES | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
| AUTHOR | | CHECKED BY | |
| Tony Tran | | Derek Huang | |
| Tue Apr 20 12:38:25 2010 | | | SHEET 28 OF 41 |



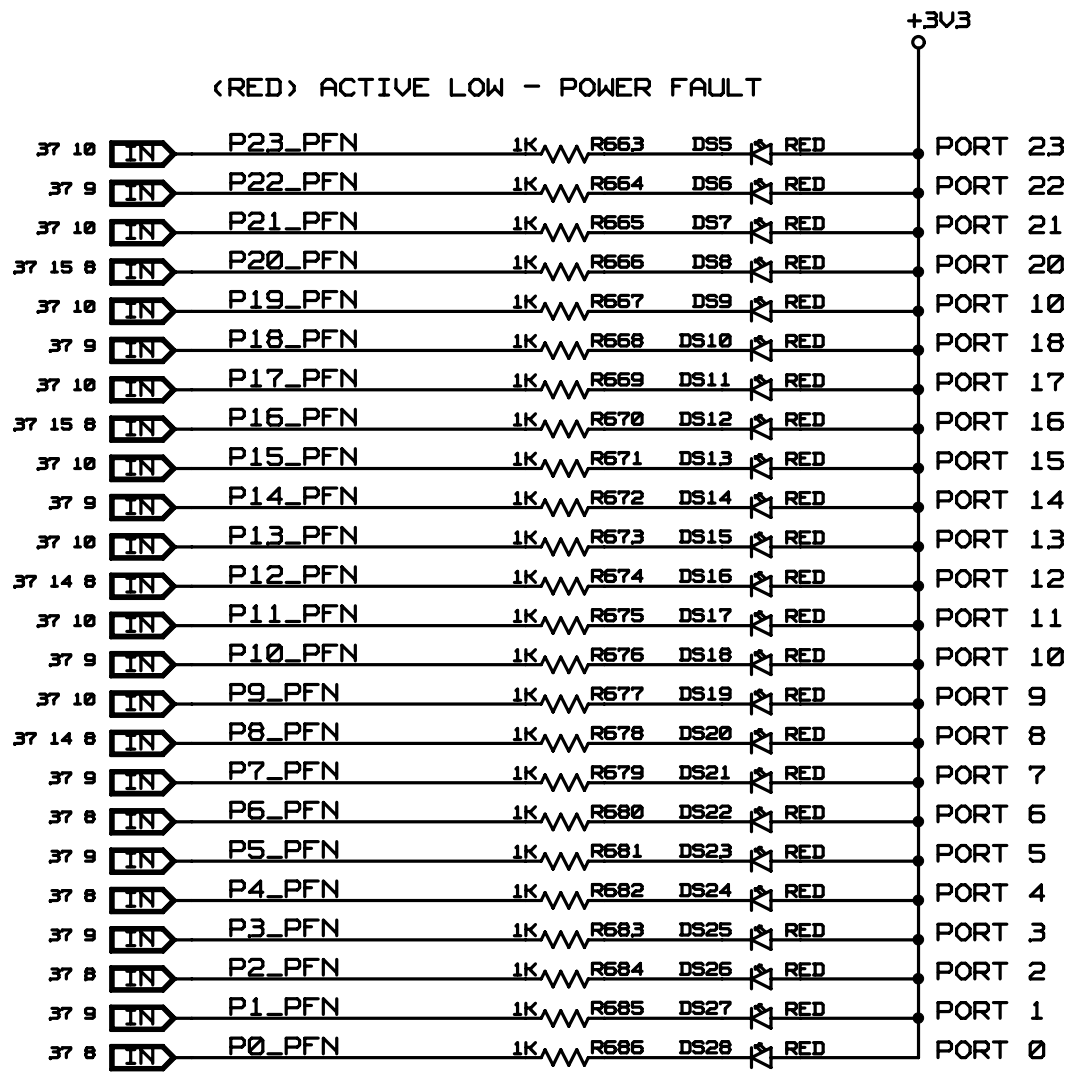
| GPIO | ALT0 | ALT1 |
|------|-------------|------------|
| 0 | PART0PERSTN | P16LINKUPN |
| 1 | PART1PERSTN | P16ACTIVEN |
| 2 | PART2PERSTN | P4LINKUPN |
| 3 | PART3PERSTN | P4ACTIVEN |
| 4 | FAILOVER0 | P0LINKUPN |
| 5 | GPEN | P0ACTIVEN |
| 7 | FAILOVER2 | P8LINKUPN |
| 8 | IOEXPINTN | P8ACTIVEN |



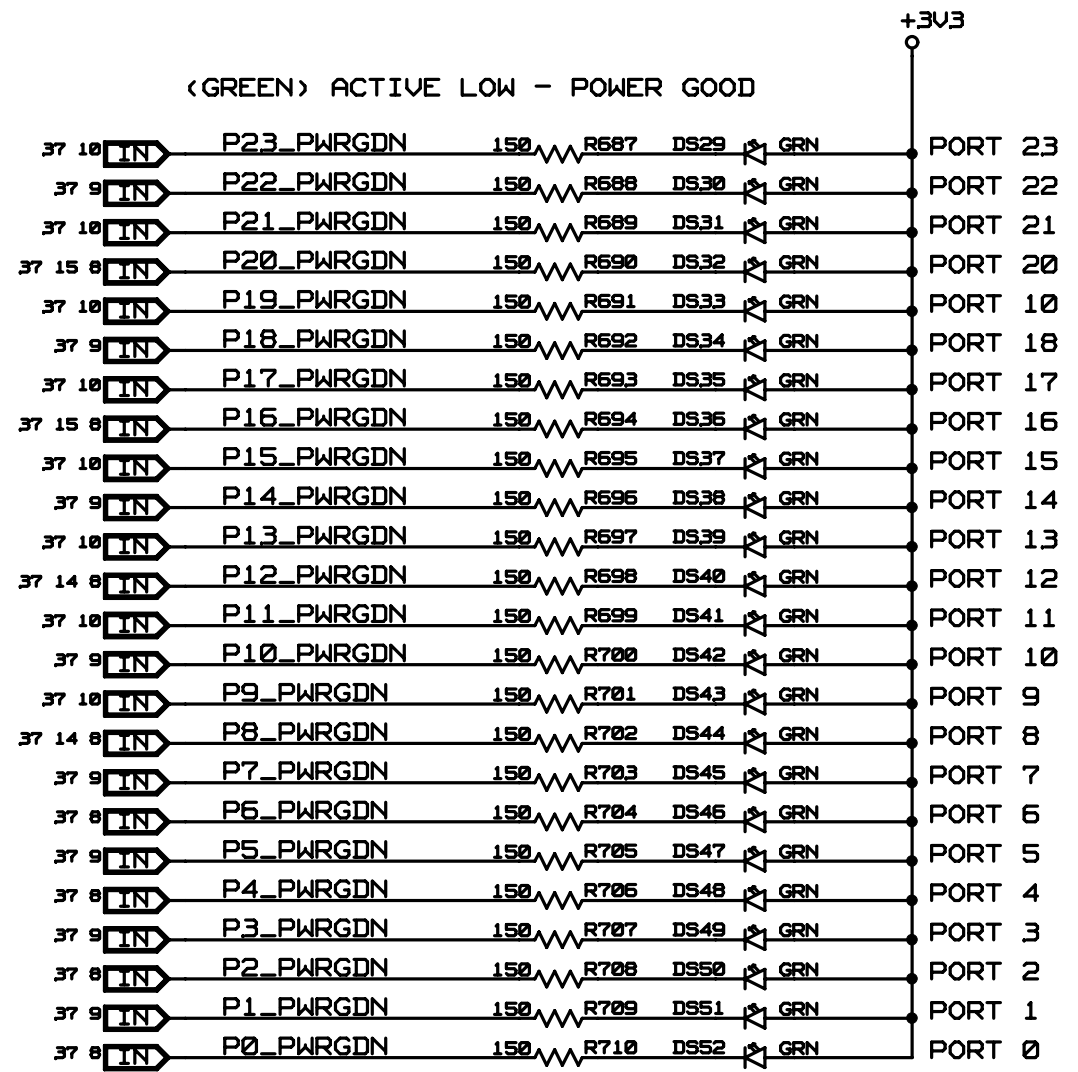
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| | | | |
|----------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS (1 OF 7) | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:25 2010 | | | SHEET 29 OF 41 |

<RED> ACTIVE LOW - POWER FAULT

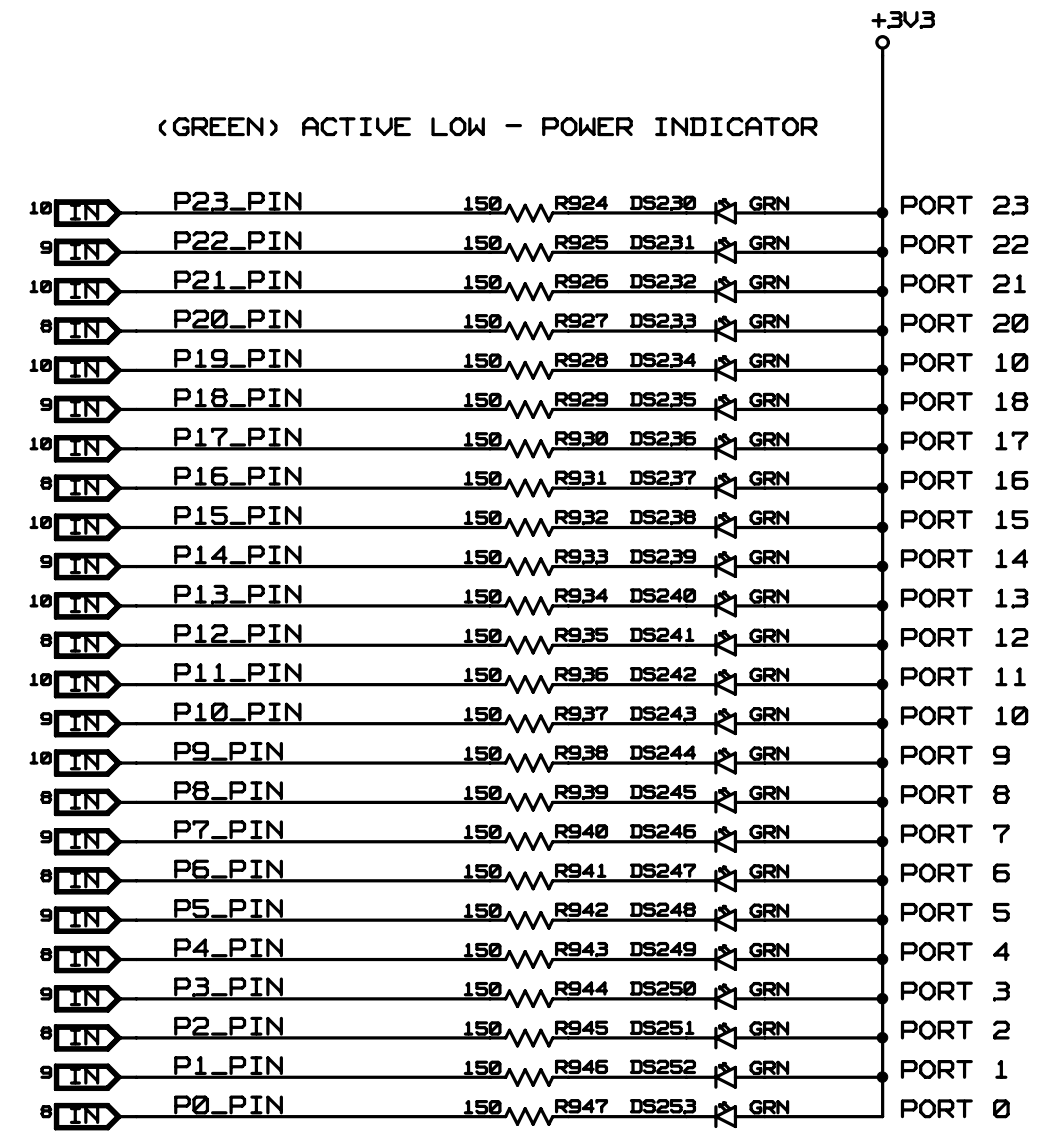
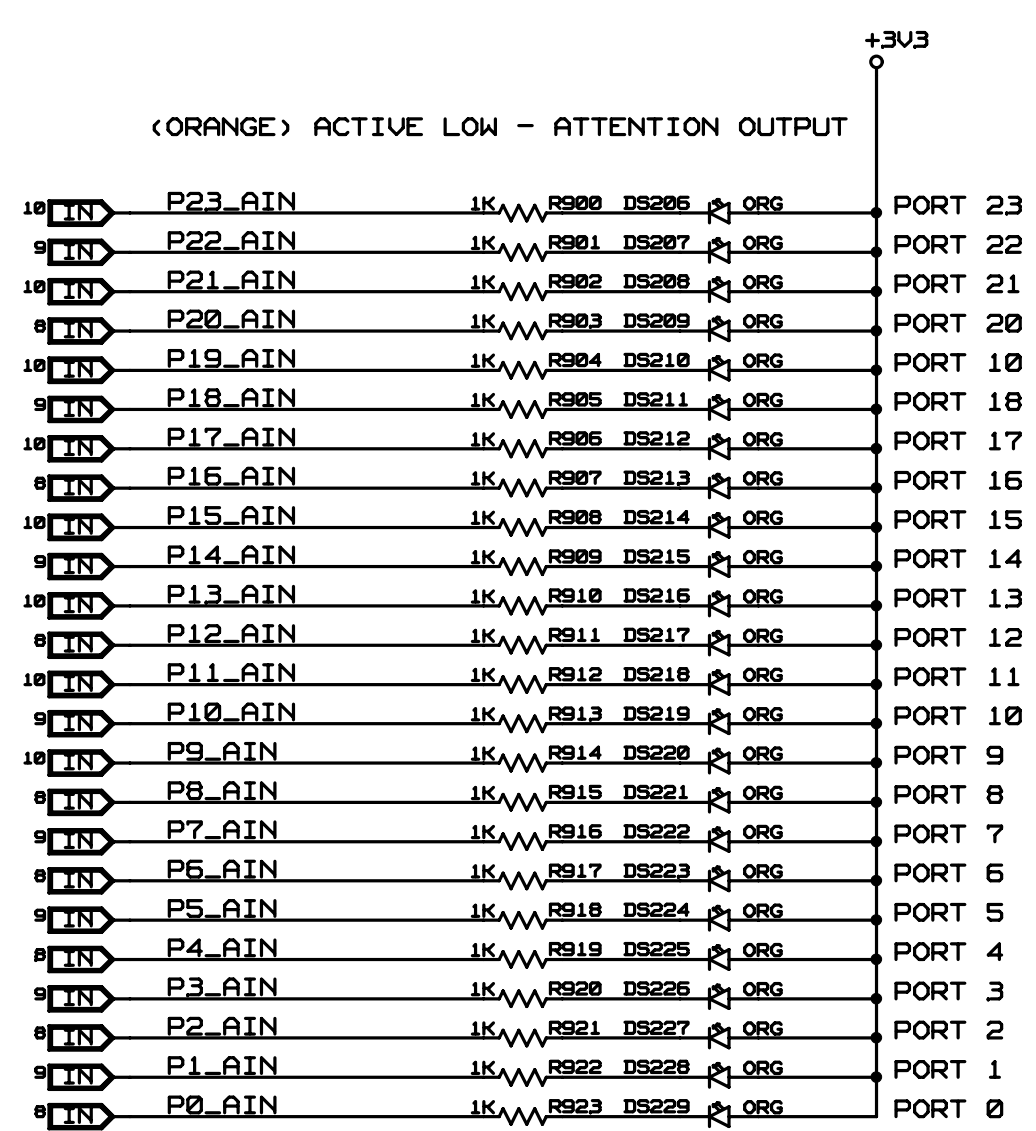


<GREEN> ACTIVE LOW - POWER GOOD



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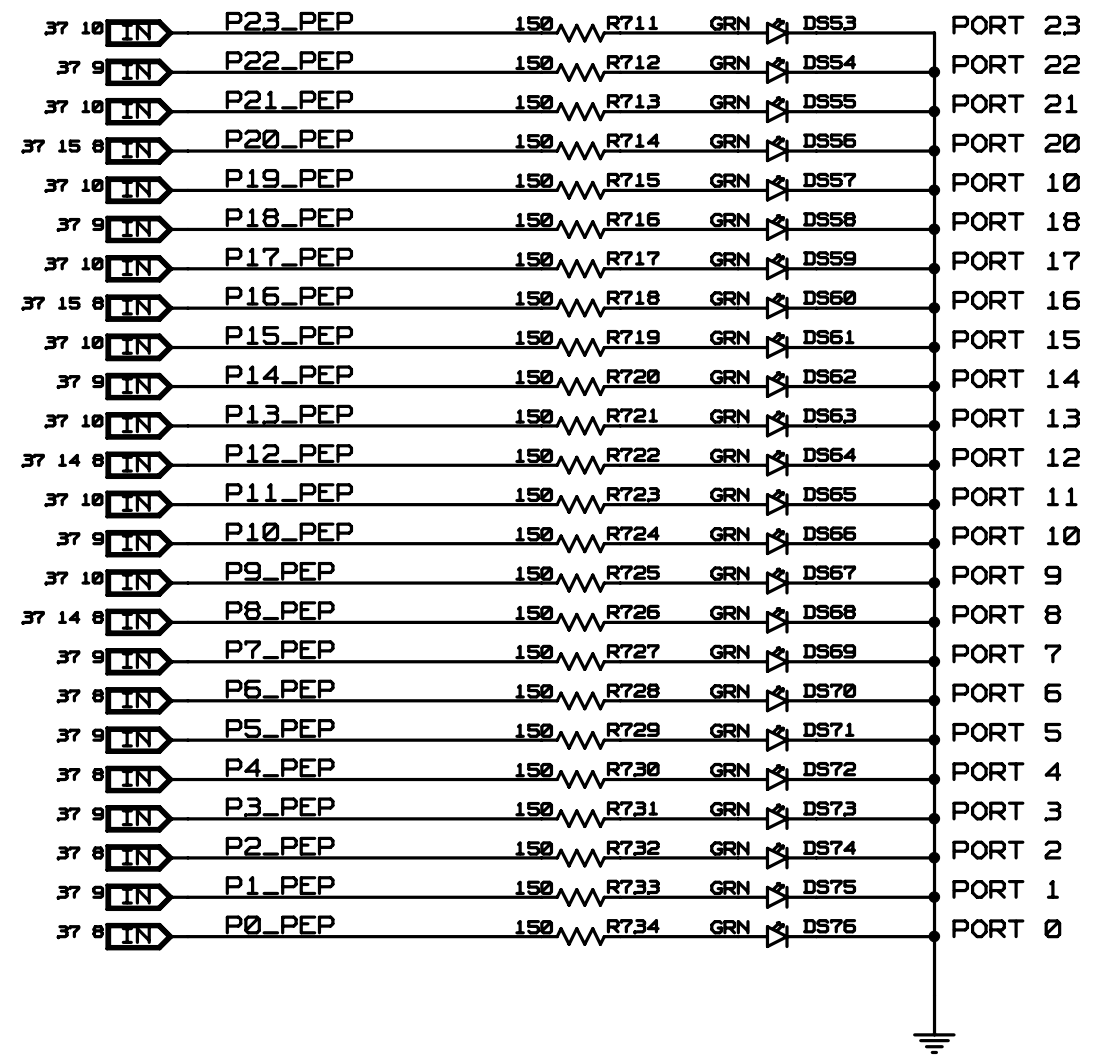
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|----------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS (2 OF 7) | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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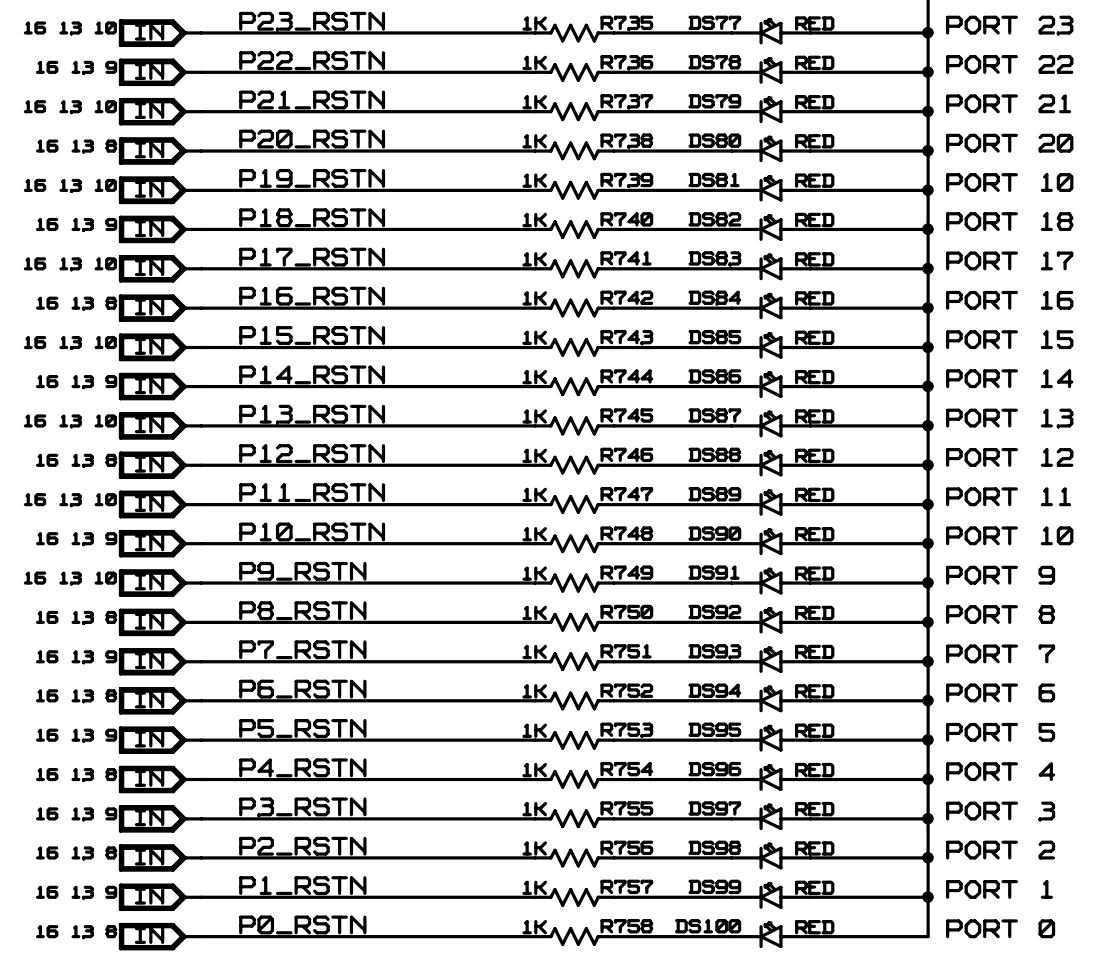
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| | | | |
|----------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS (3 OF 7) | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:27 2010 | | | SHEET 31 OF 41 |

<GREEN> ACTIVE HIGH - POWER ENABLE



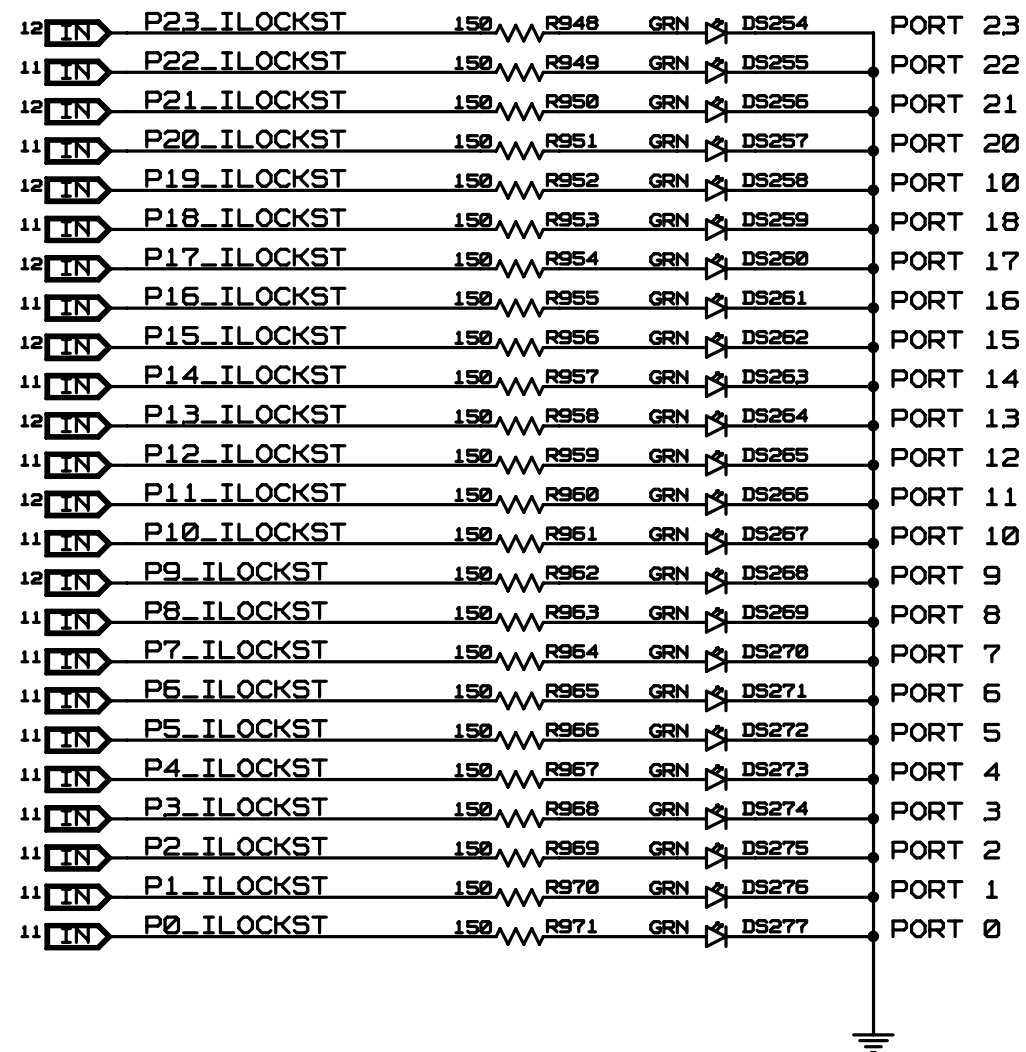
<RED> ACTIVE LOW - HP SLOT RST



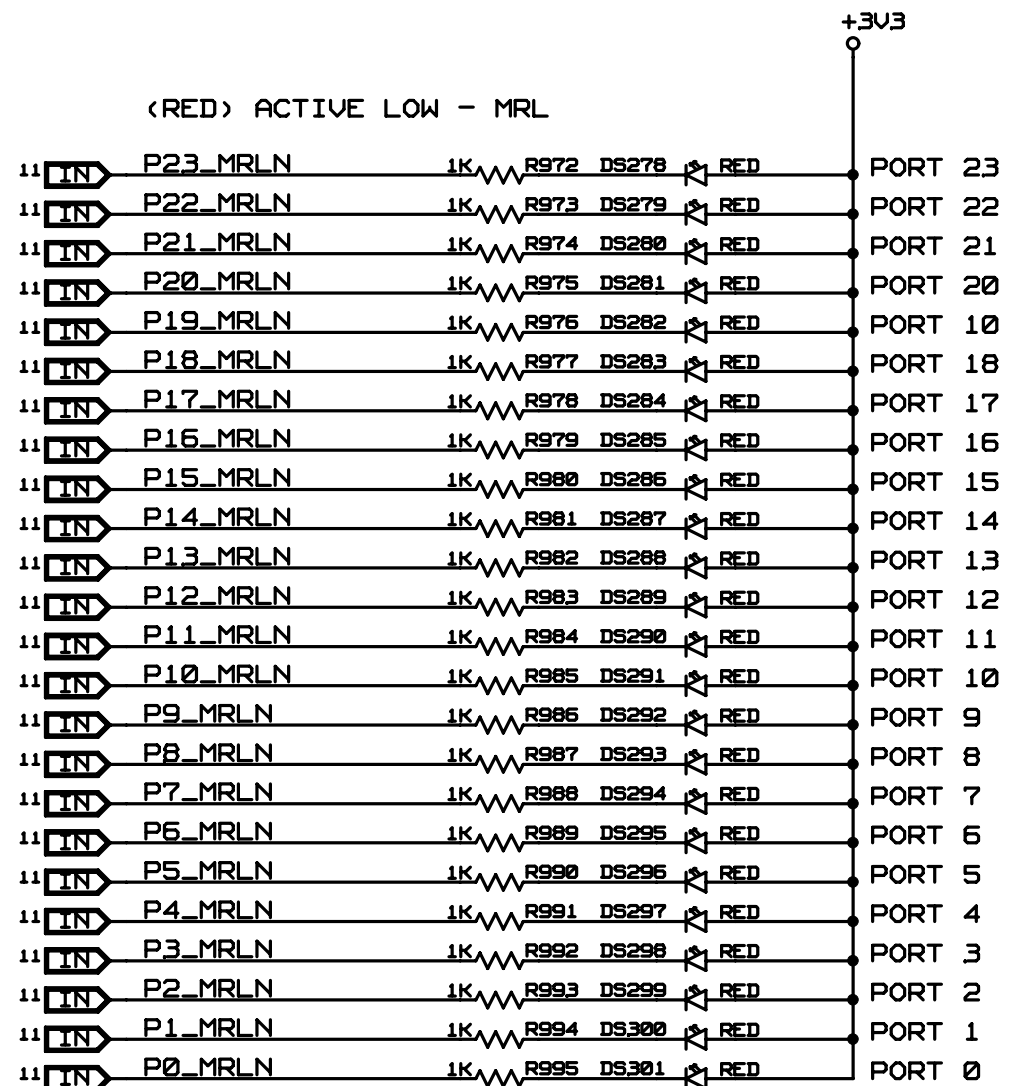
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| | | | |
|------------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS < 4 OF 7 > | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:28 2010 | | | SHEET 32 OF 41 |

<GREEN> ACTIVE HIGH - INTERLOCK INPUT



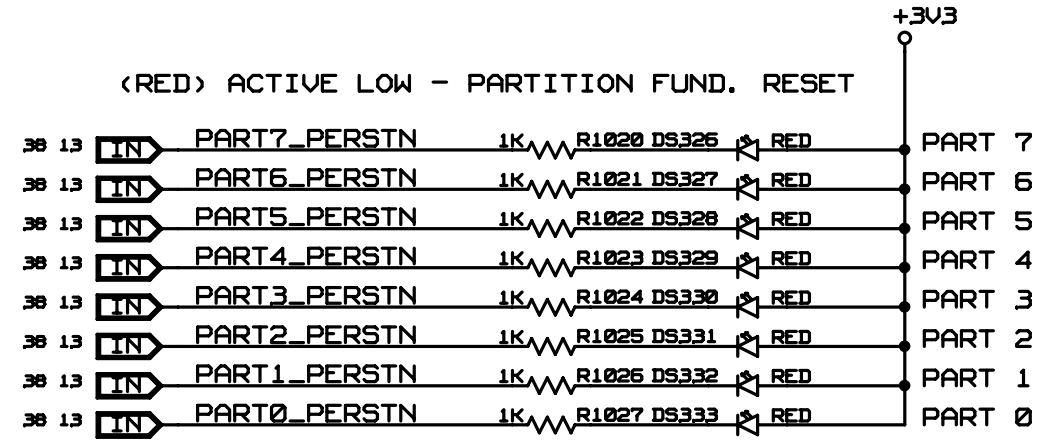
<RED> ACTIVE LOW - MRL



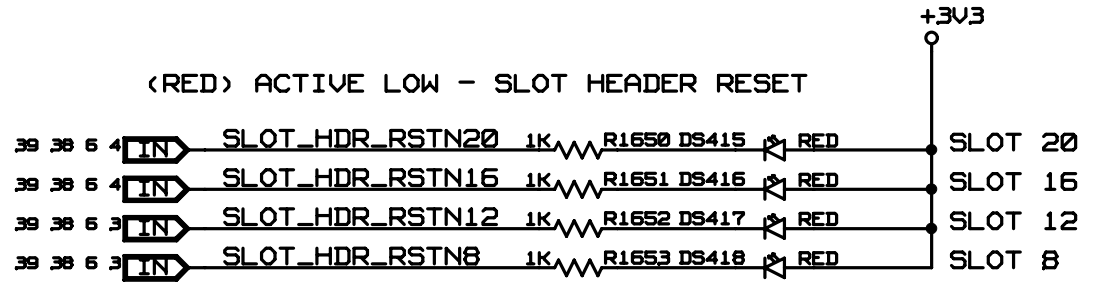
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| | | | |
|----------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS <5 OF 7> | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:28 2010 | | | SHEET 33 OF 41 |

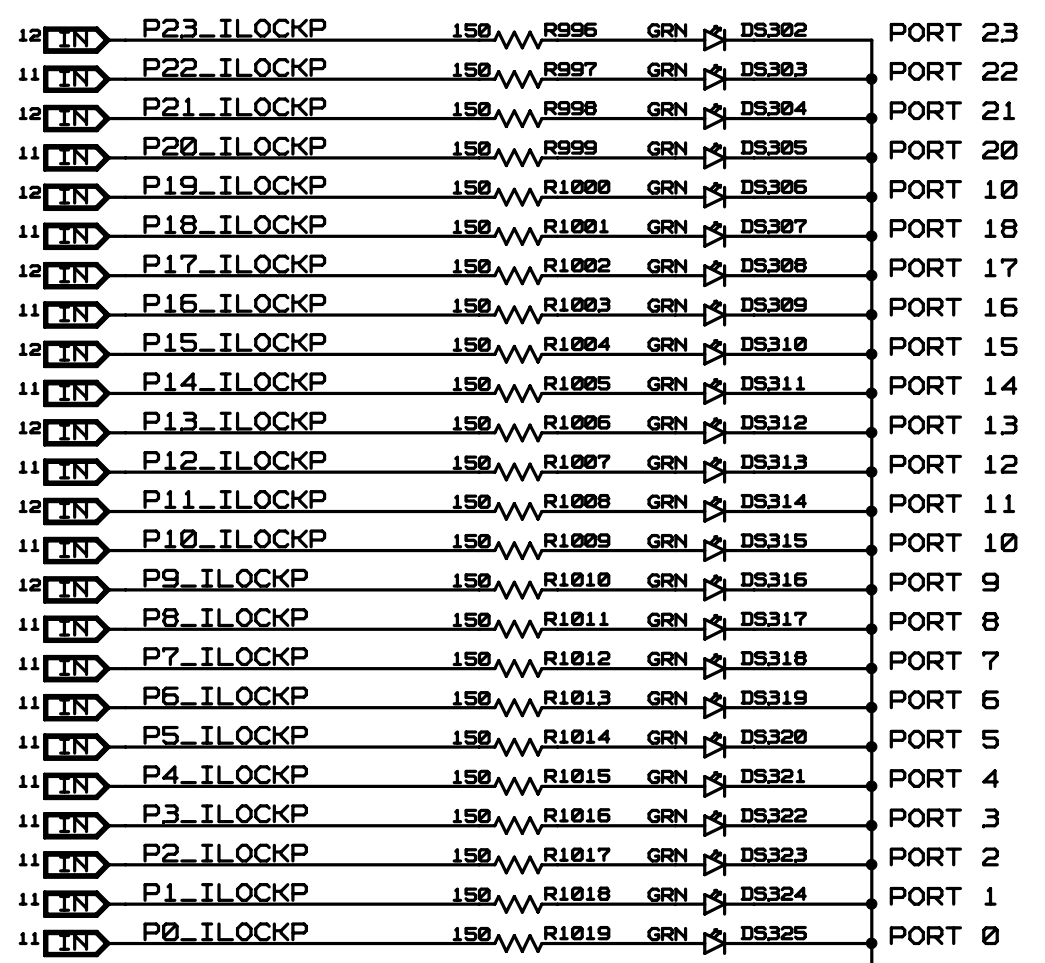
<RED> ACTIVE LOW - PARTITION FUND. RESET



<RED> ACTIVE LOW - SLOT HEADER RESET

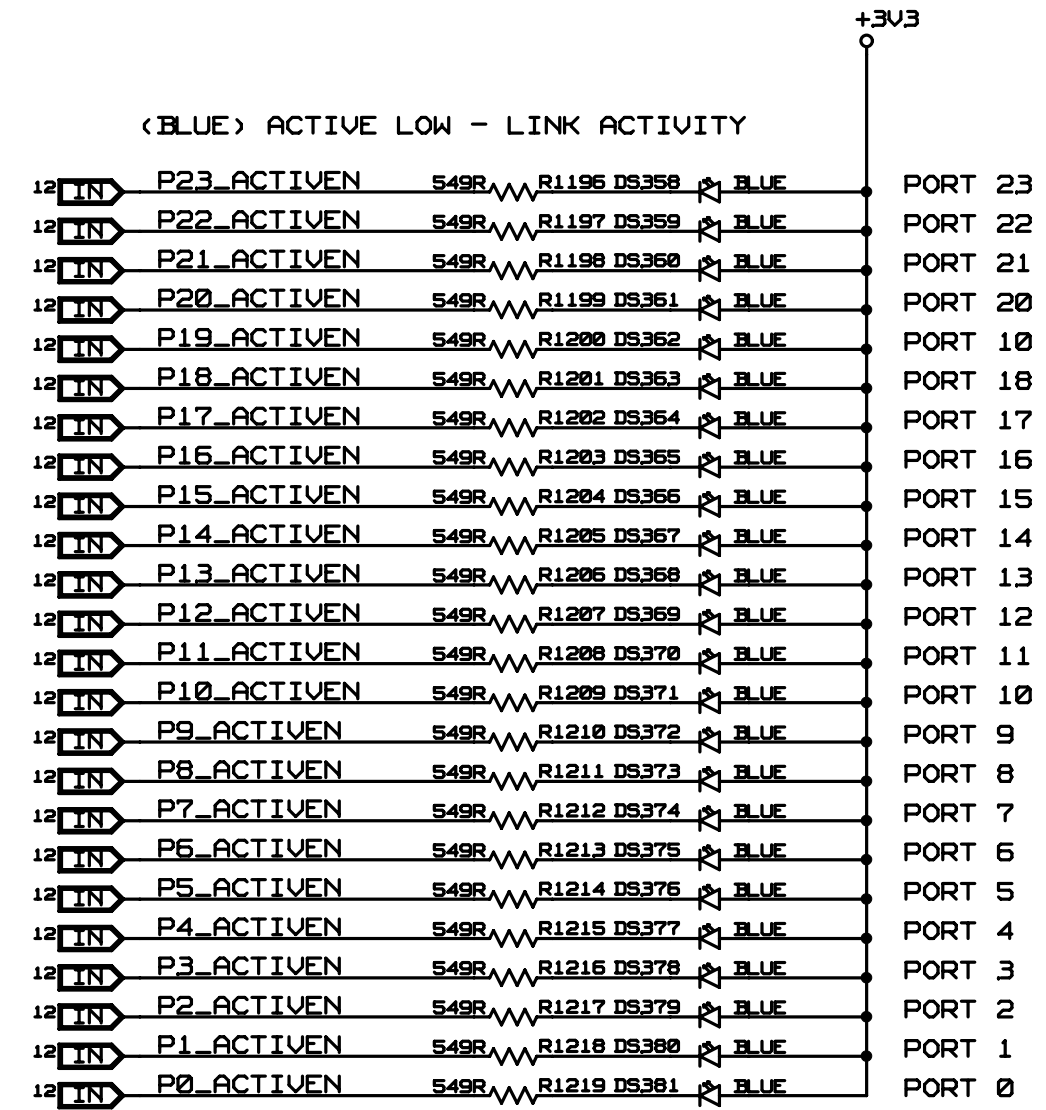
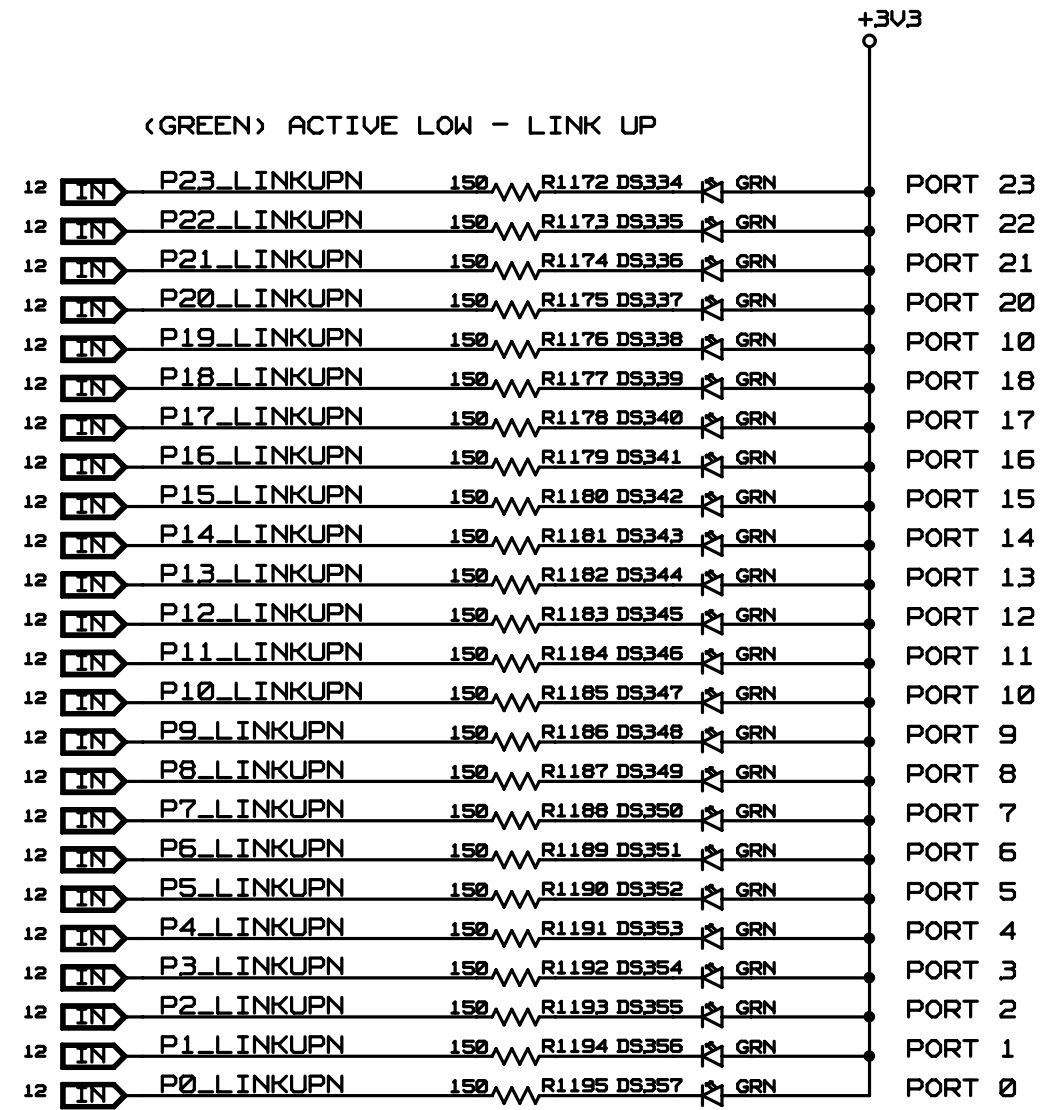


<GREEN> ACTIVE HIGH - INTERLOCK OUTPUT



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| | | | |
|----------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS <6 OF 7> | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:28 2010 | | | SHEET 34 OF 41 |

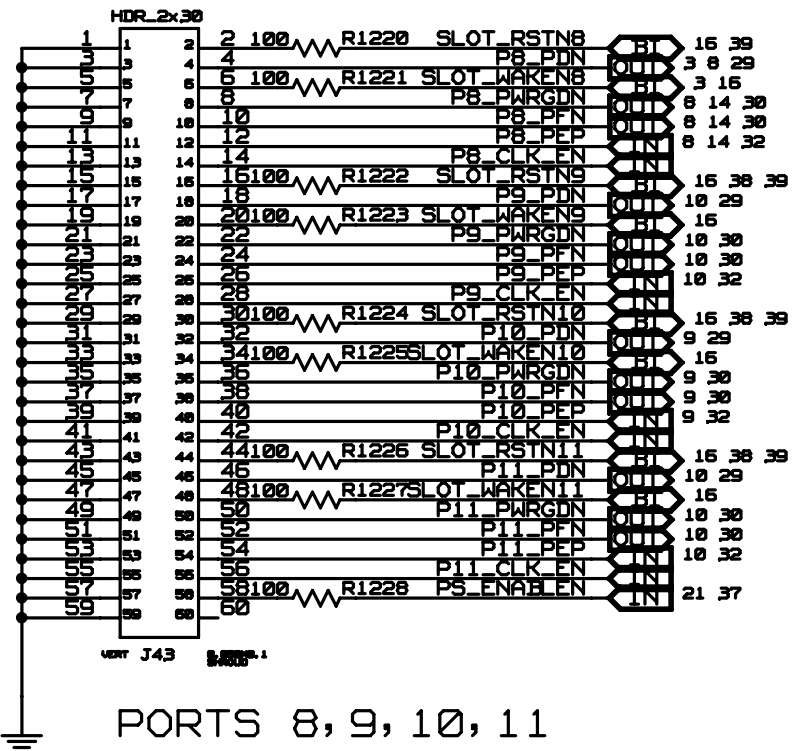


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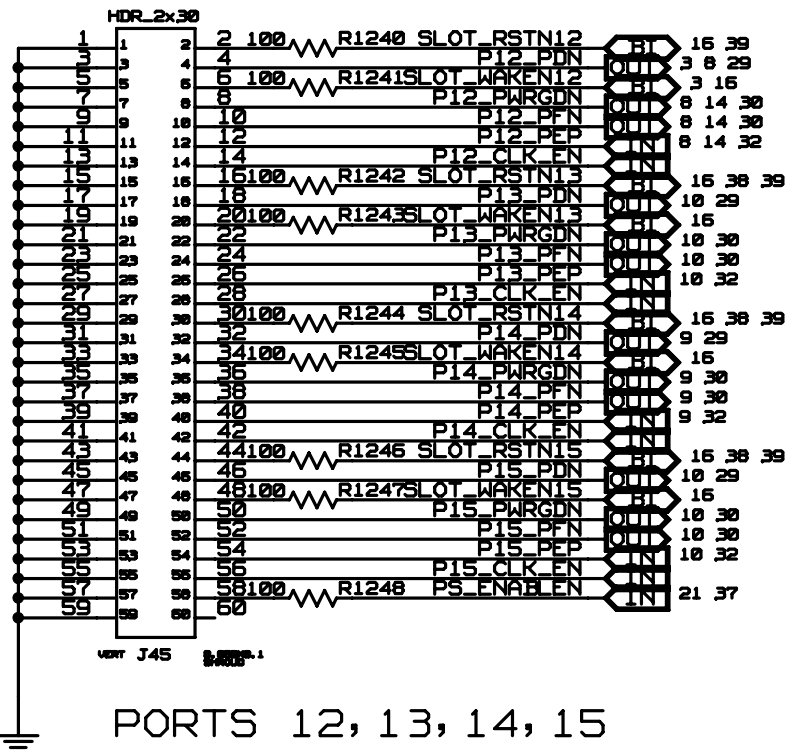
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|------------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| LED - PORT STATUS (<7 OF 7>) | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
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SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

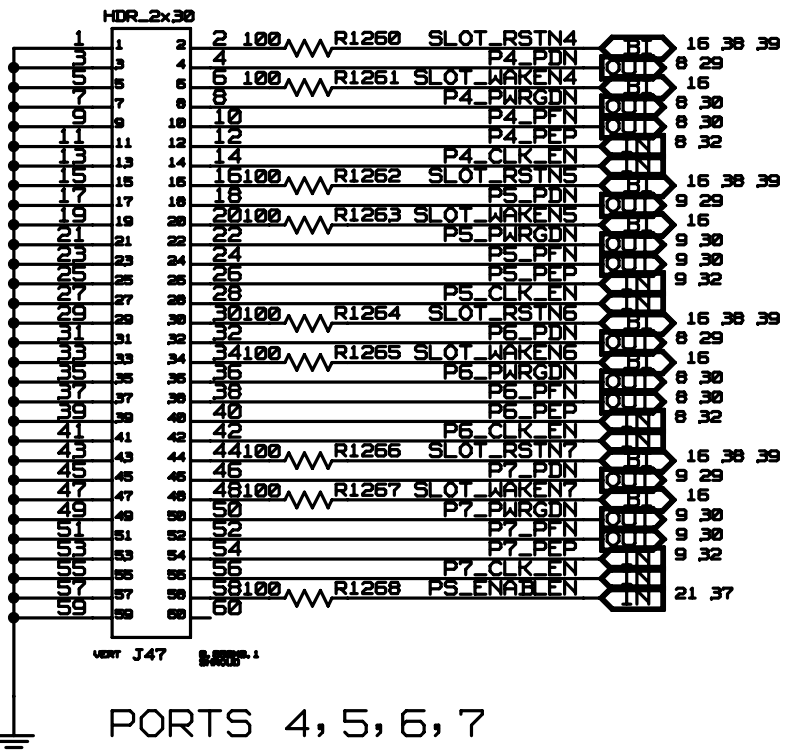
PS_ENABLEN
CABLE SENSE



PORTS 8, 9, 10, 11



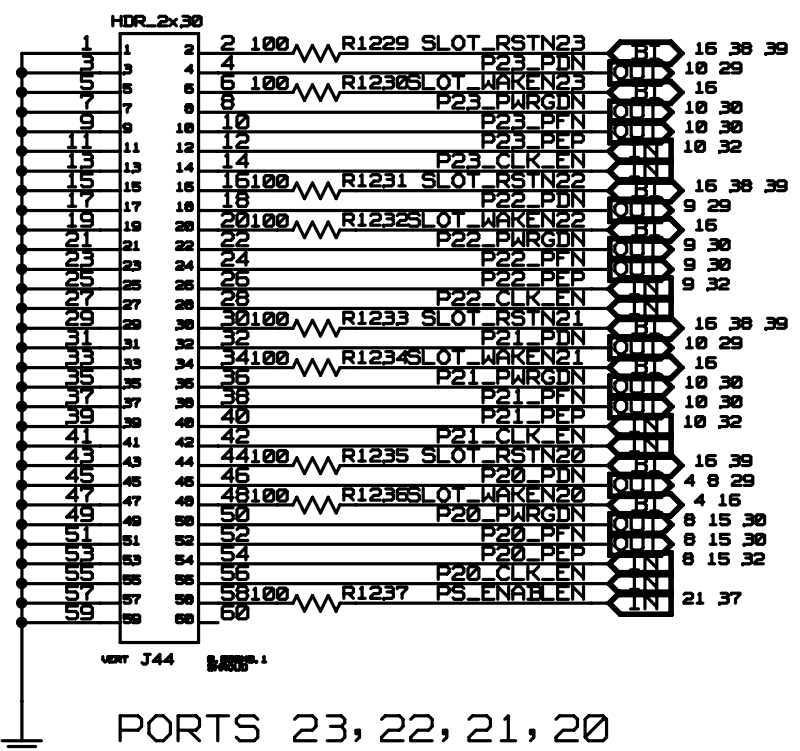
PORTS 12, 13, 14, 15



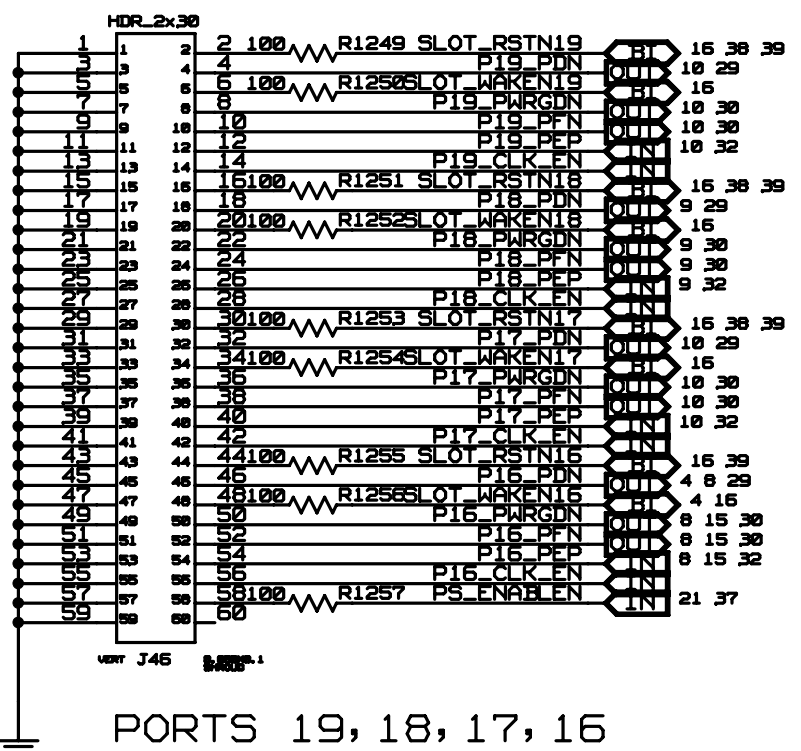
PORTS 4, 5, 6, 7

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN

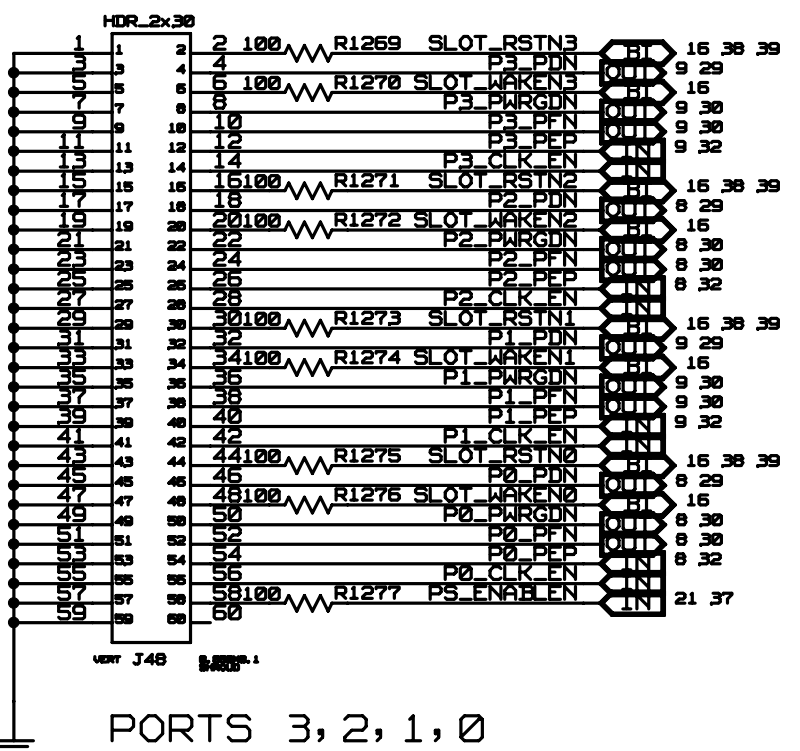
PS_ENABLEN
CABLE SENSE



PORTS 23, 22, 21, 20

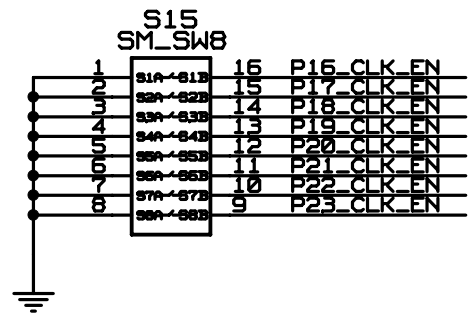
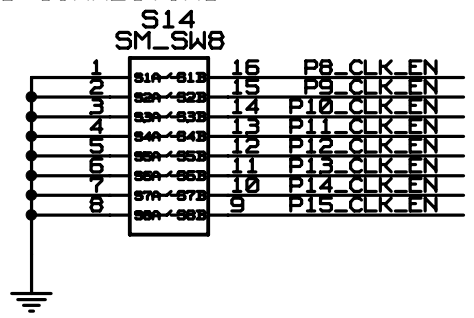
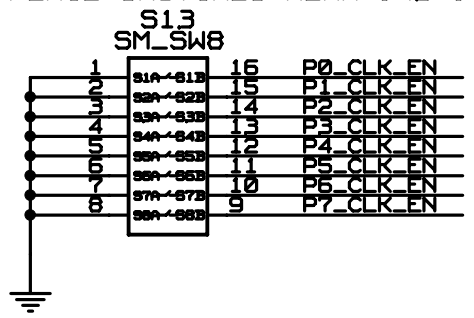


PORTS 19, 18, 17, 16



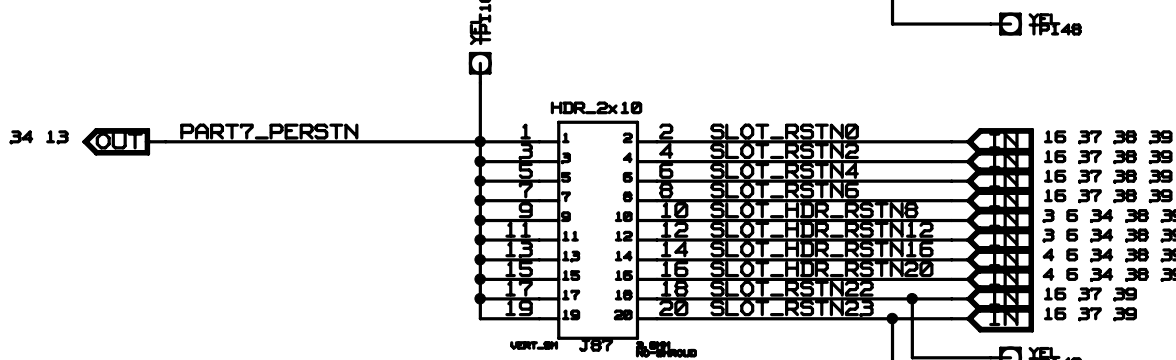
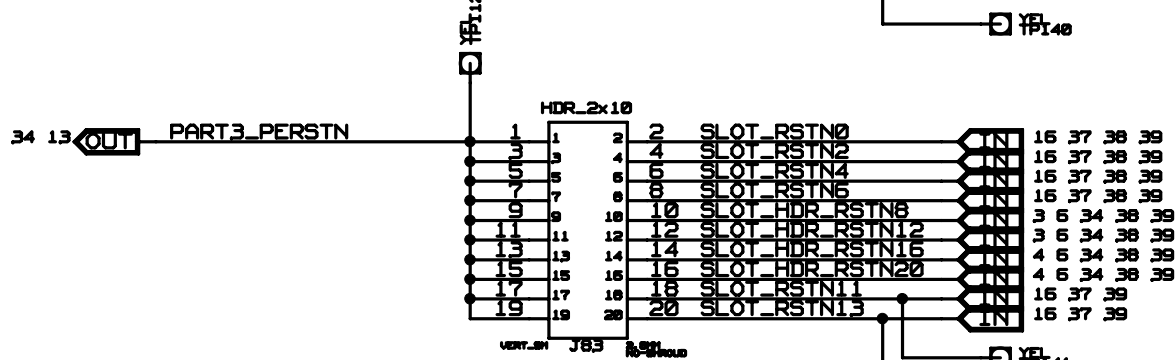
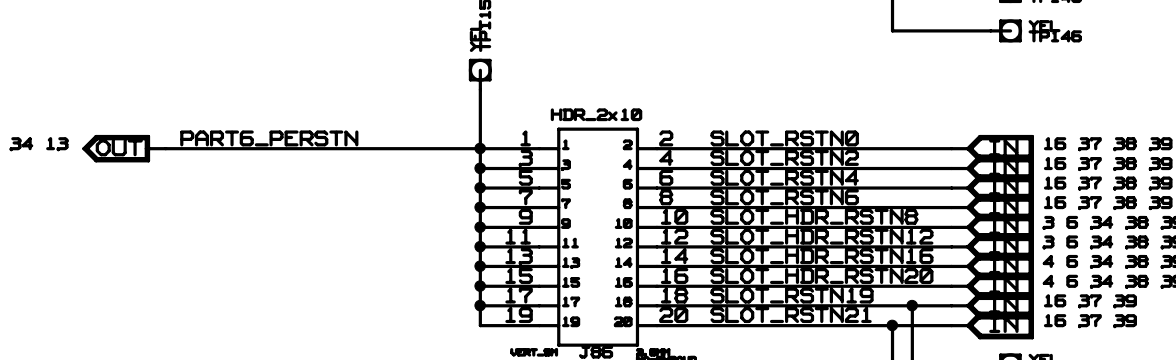
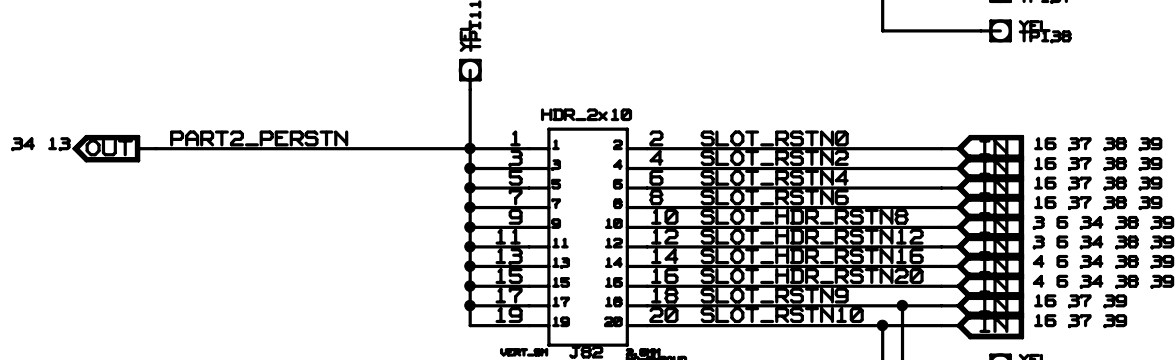
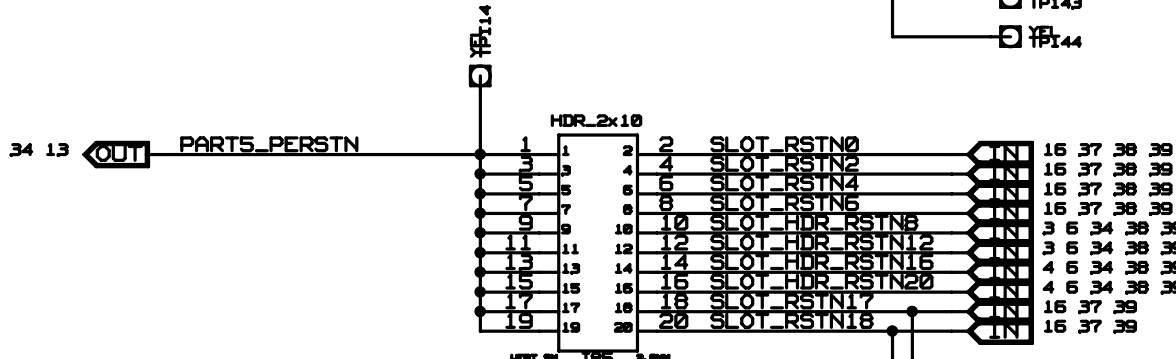
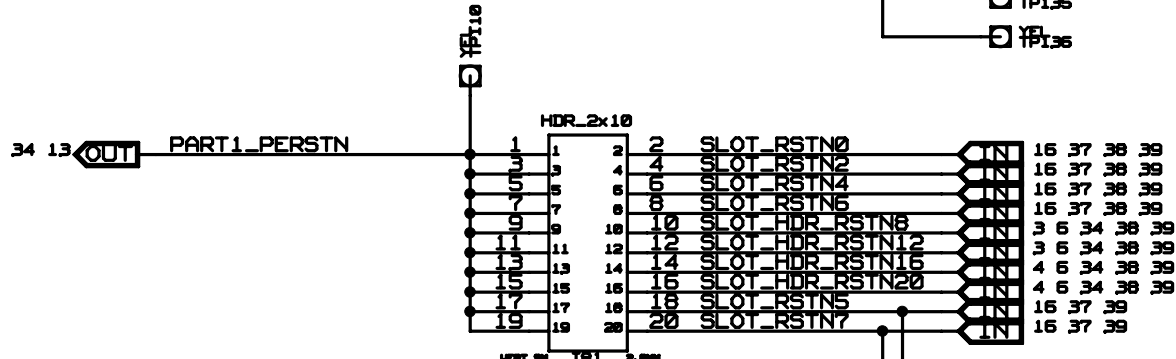
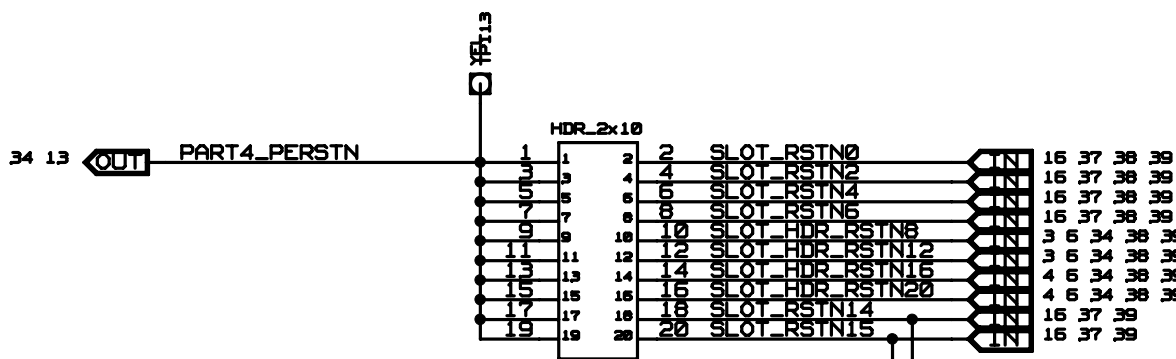
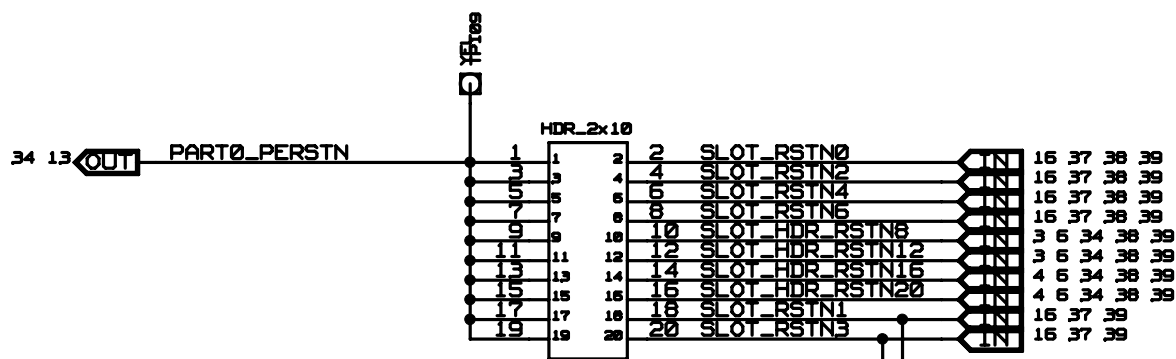
PORTS 3, 2, 1, 0

PLACE SWITCHES NEAR J43-J48 CONNECTORS



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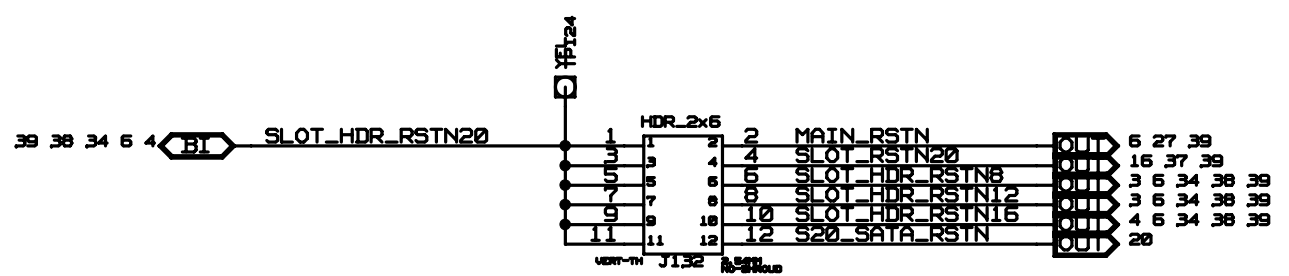
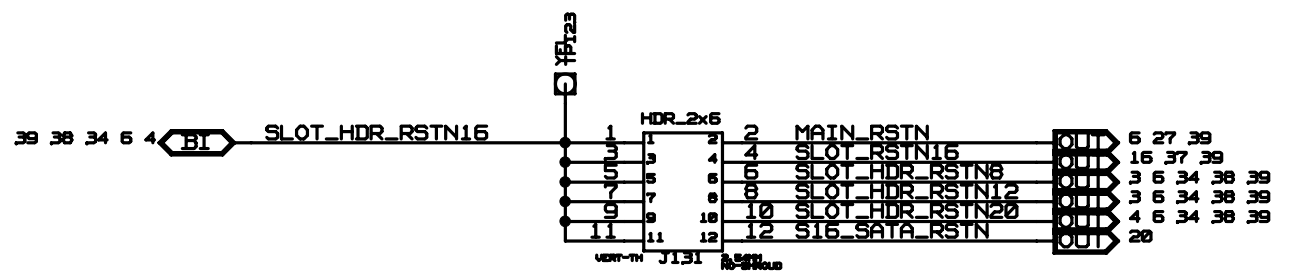
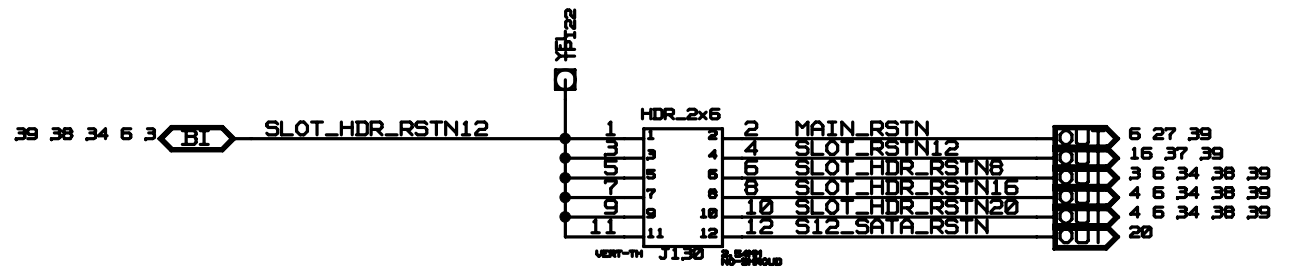
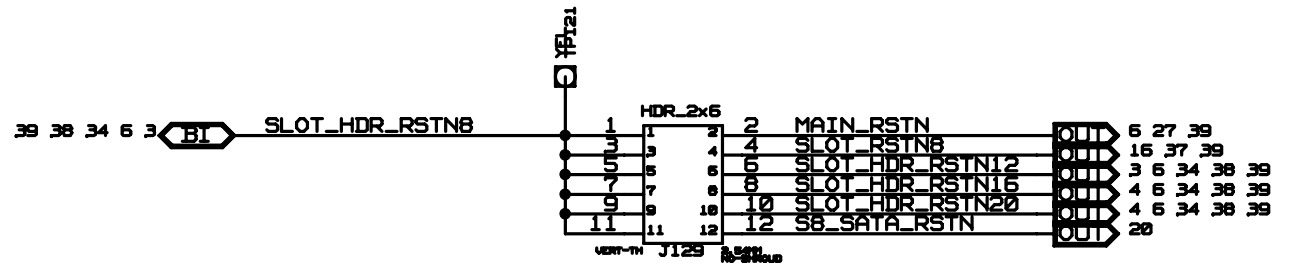
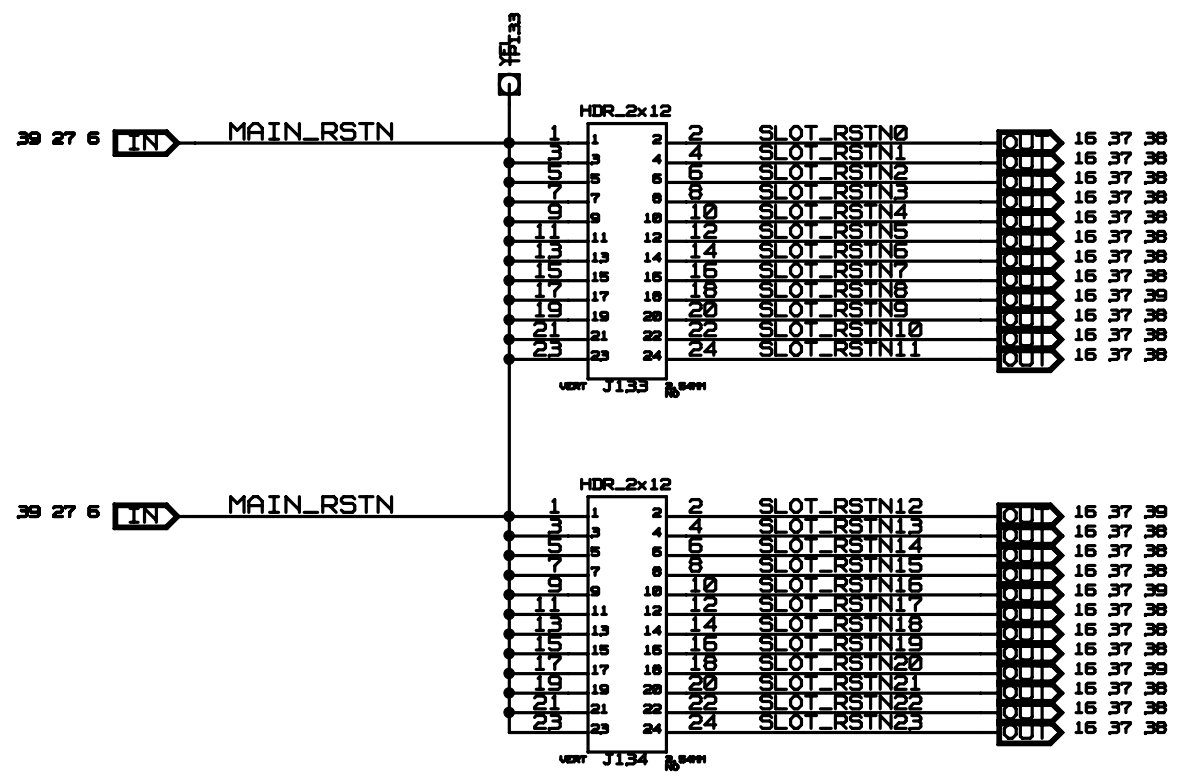
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| TITLE EB-LOGAN-19 | | | |
| SIDEBAND CONNECTORS | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
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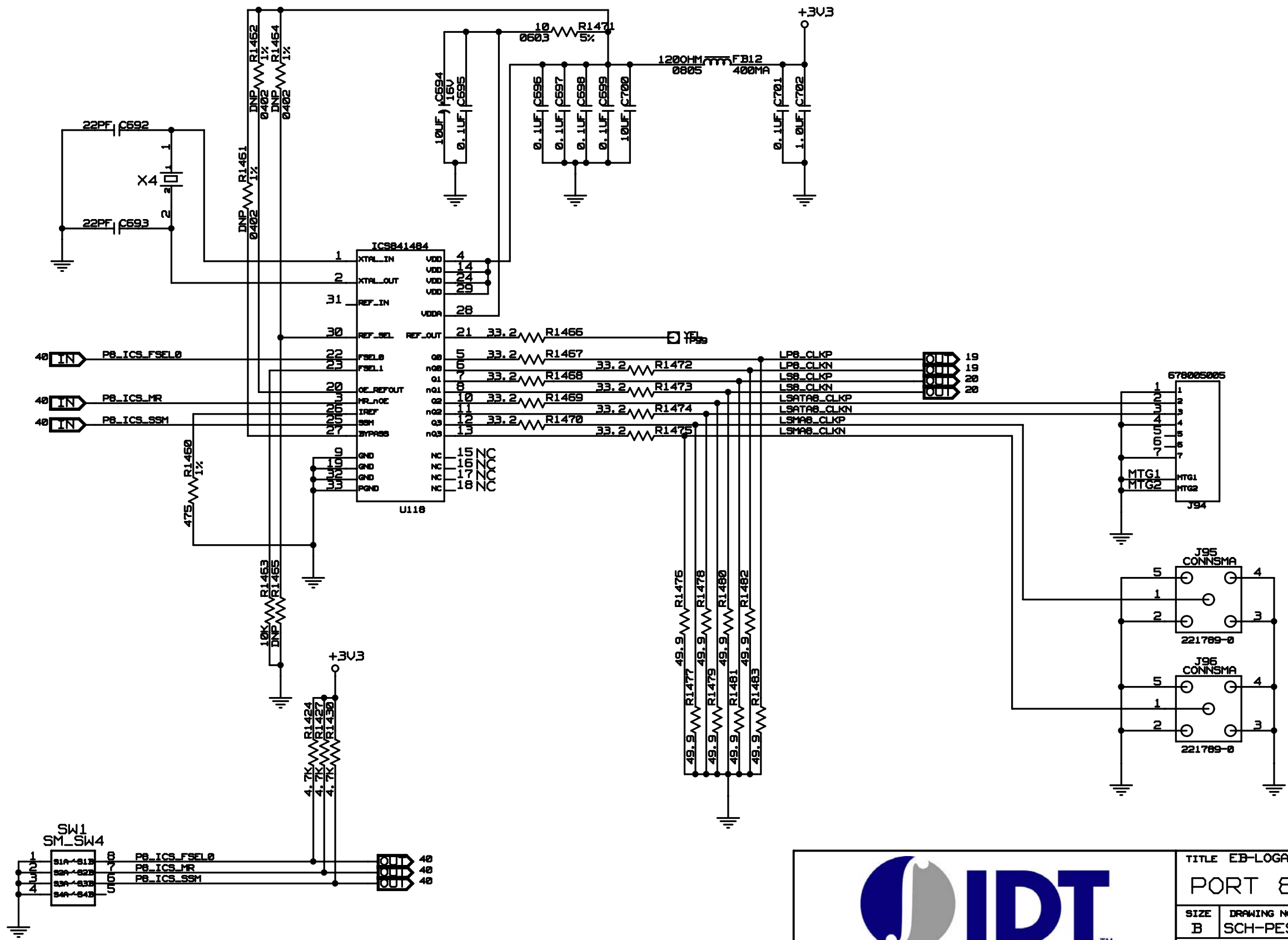

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| TITLE EB-LOGAN-19 | | | |
| PARTITION RESET SELECT HEADERS | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
| AUTHOR | | CHECKED BY | |
| Tony Tran | | Derek Huang | |
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NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED



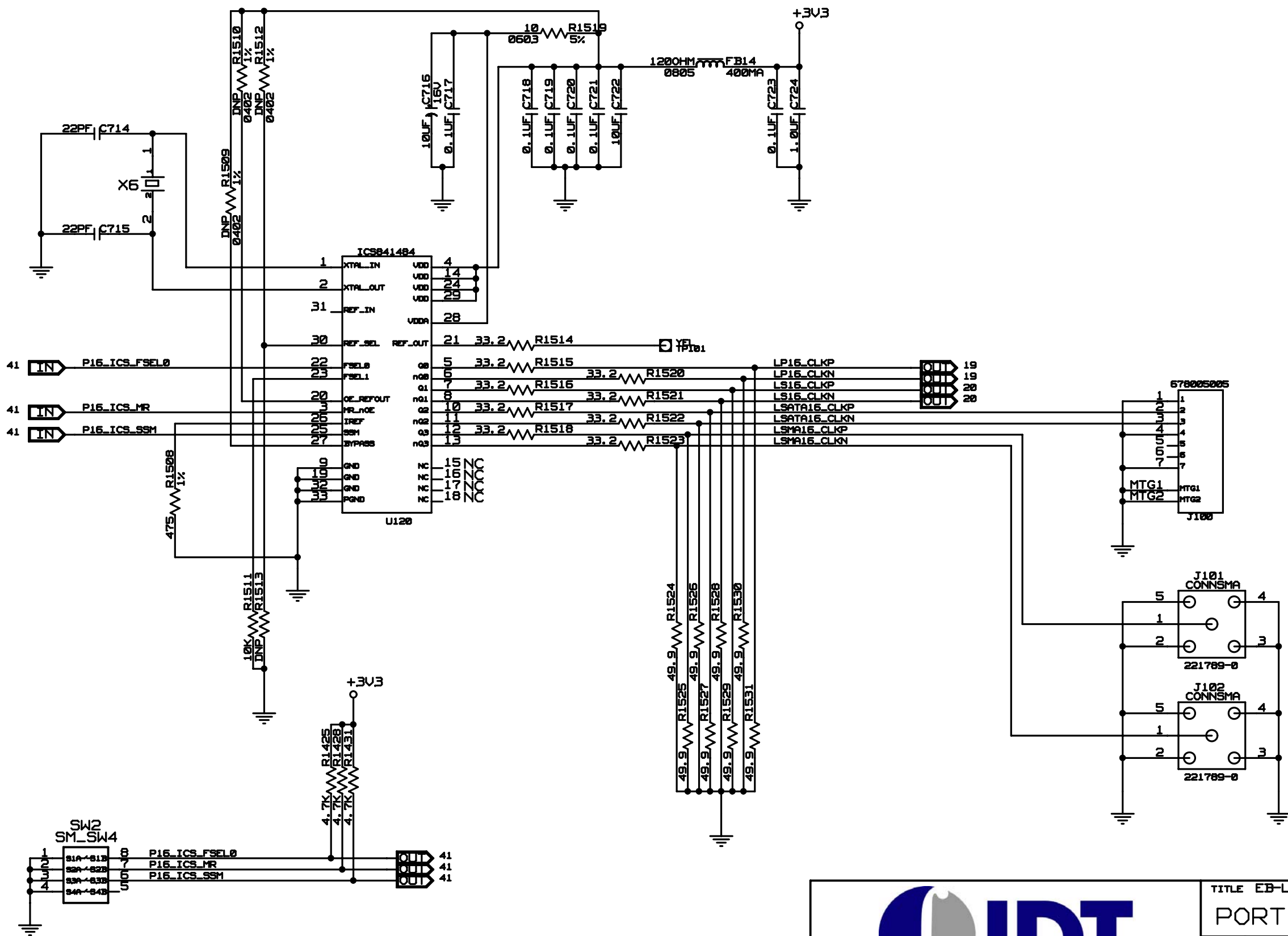
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| | | | |
|---------------------------|---------------|-------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| SLOT RESET SELECT HEADERS | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
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| | | | |
|--------------------------|---------------|-------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| PORT 8 CLOCK GENERATOR | | | |
| SIZE | DRAWING NO. | FAB P/N | REV. |
| B | SCH-PESEB-002 | 18-692-000 | 1.1 |
| AUTHOR | | CHECKED BY | |
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| | | | |
|--------------------------|------------------------------|---------------------------|----------------|
| TITLE EB-LOGAN-19 | | | |
| PORT 16 CLOCK GENERATOR | | | |
| SIZE B | DRAWING NO. SCH-PESEB-002 | FAB P/N 18-692-000 | REV. 1.1 |
| AUTHOR Tony Tran | | CHECKED BY Derek Huang | |
| Tue Apr 20 12:38:31 2010 | | | SHEET 41 OF 41 |