

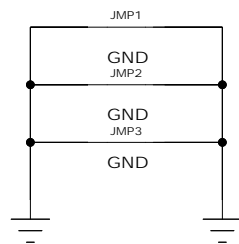
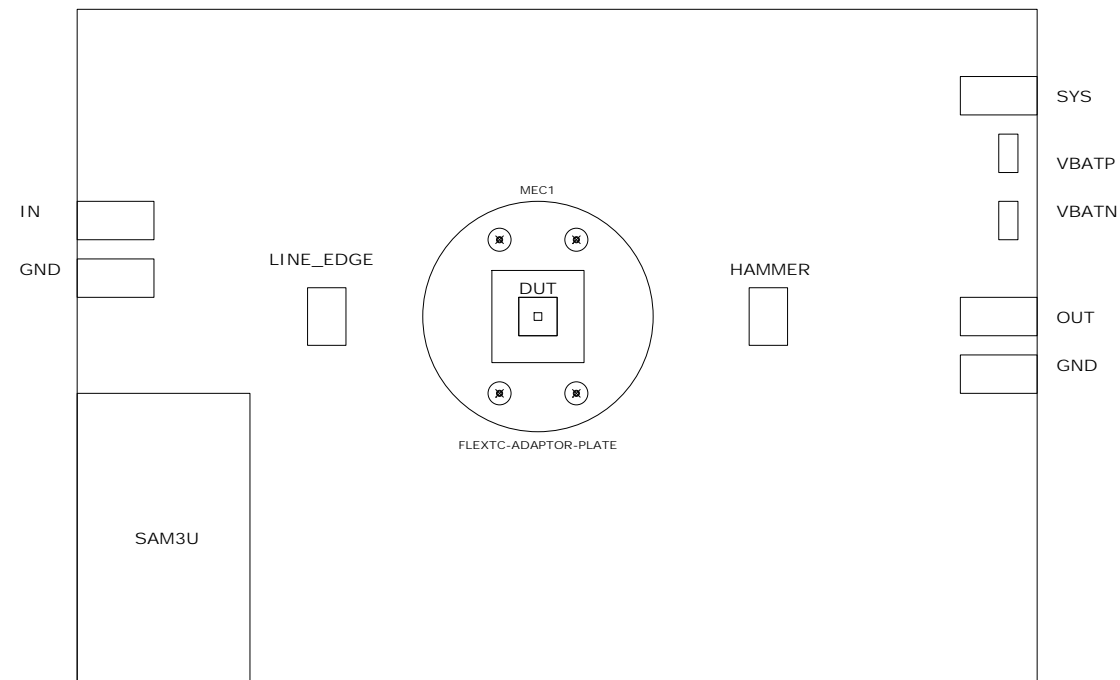
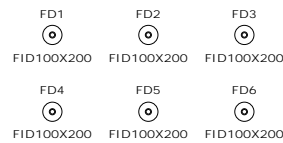
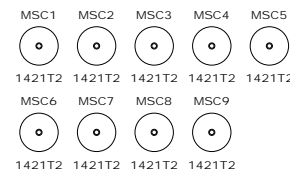
REVISION TABLE

REV.	DATE	ENGINEER	NOTES
A00	16/10/2016	GF	Initial version.
A01	17/10/2016	GC	Some refdes changed to match board i will be using as my starting point. Silkscreen label at header J7 changed to OUT. Silkscreen label at header J3 changed to IN. Silkscreen labels added at RF connectors. Two single blue jumper links removed at headers J18 & J19 and replaced with one double black jumper link. Two single blue jumper links removed at header J22 and replaced with one double black jumper link.
A02	25/10/2016	GC	1x2 header J7 removed. RF connectors J35, J52, J53 changed to Unpop. Resistors R46, R47, R60 changed to Unpop.
A03	09/01/2017	GF	Added a clarifying note on page 1, explaining that C1M/C2M are used interchangeably with C1N/C2N.

MECHANICAL PARTS

NOTE: C1M = C1N
C2M = C2N

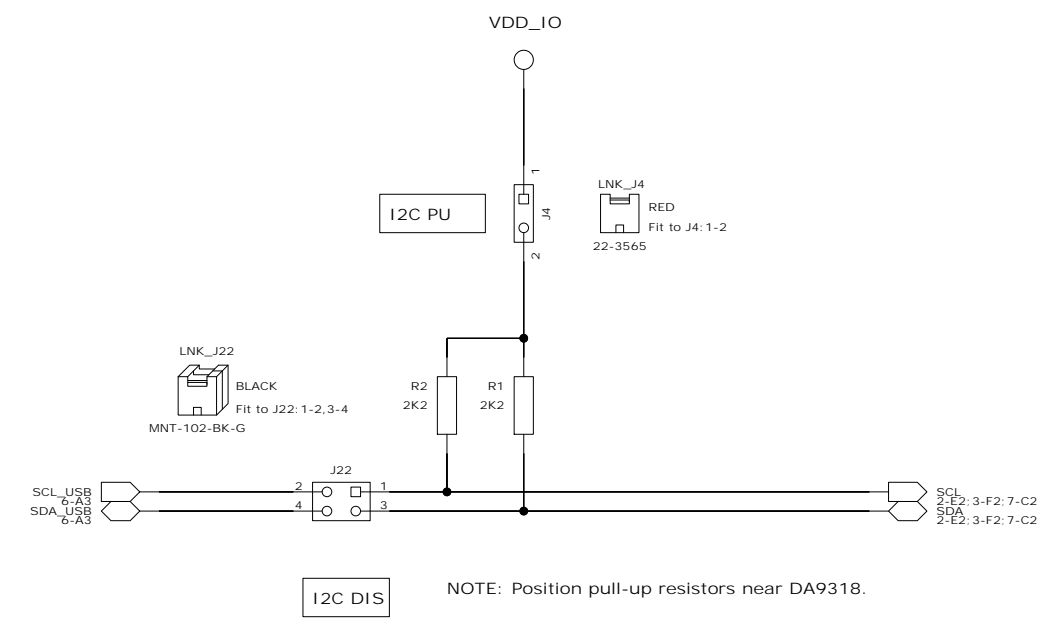
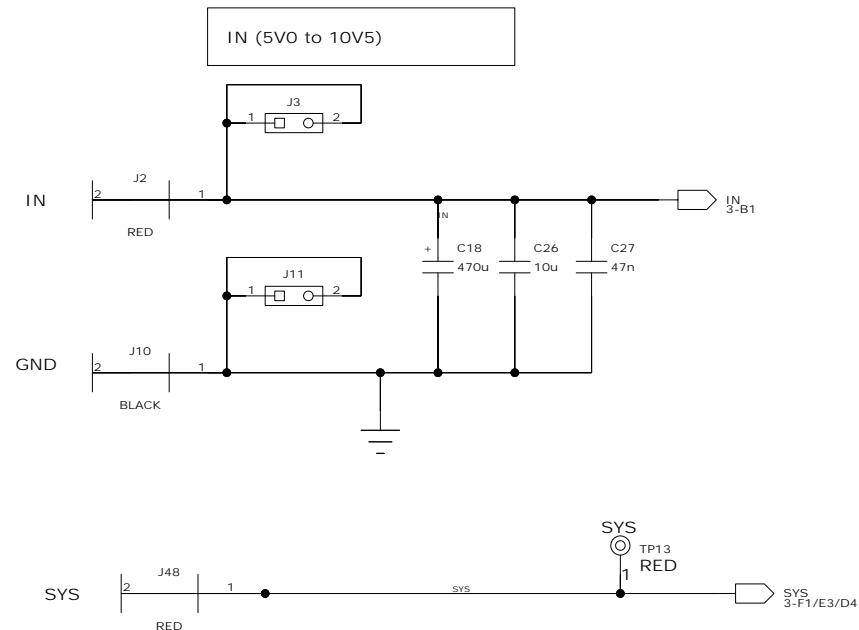
MECHANICAL



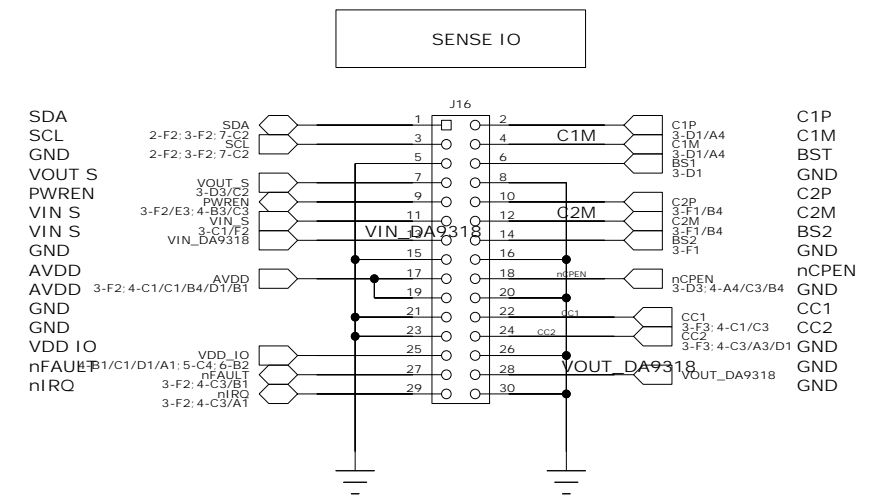
LAYOUT NOTE: SPREAD GND LOOPS EVENLY AROUND THE BOARD.
LAYOUT NOTE: REFER TO REDWOOD_RECOMMENDED_LAYOUT.PDF

SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015) DESIGNED BY: Greg Fattig REVIEWED BY: GF, GC	CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 EVB Solder	
	SAVED DATE: 25/02/2022	DRAWING NO: 329-01-A	REV: A01	
REVIEWED DATE: 27/09/2016	SHEET NAME: REVISION		PAGE: 1 of 7	

POWER & IOs



NOTE: Position pull-up resistors near DA9318.



SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

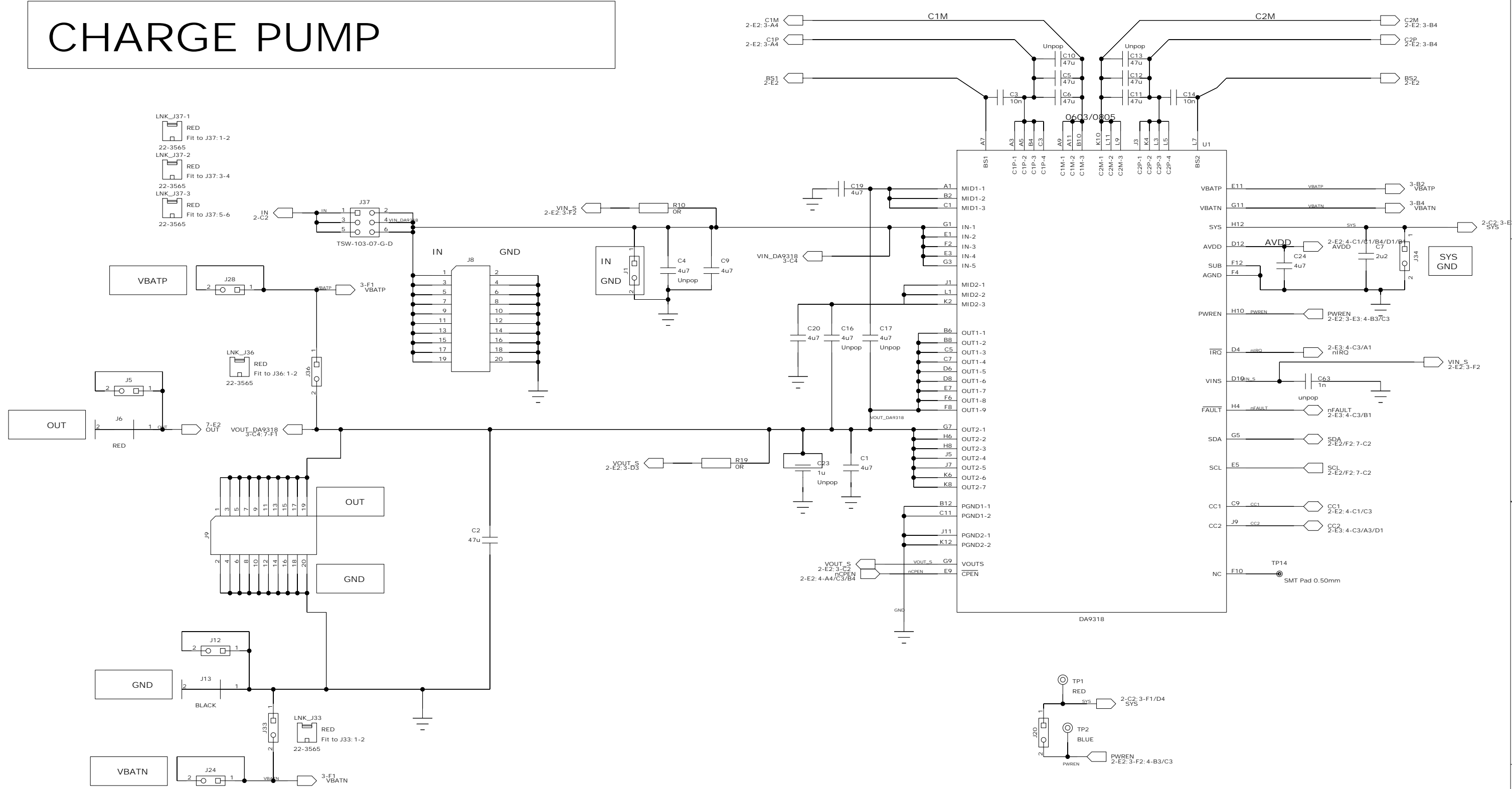
DESIGNED BY:
Greg Fattig

REVIWED BY:
GF, GC

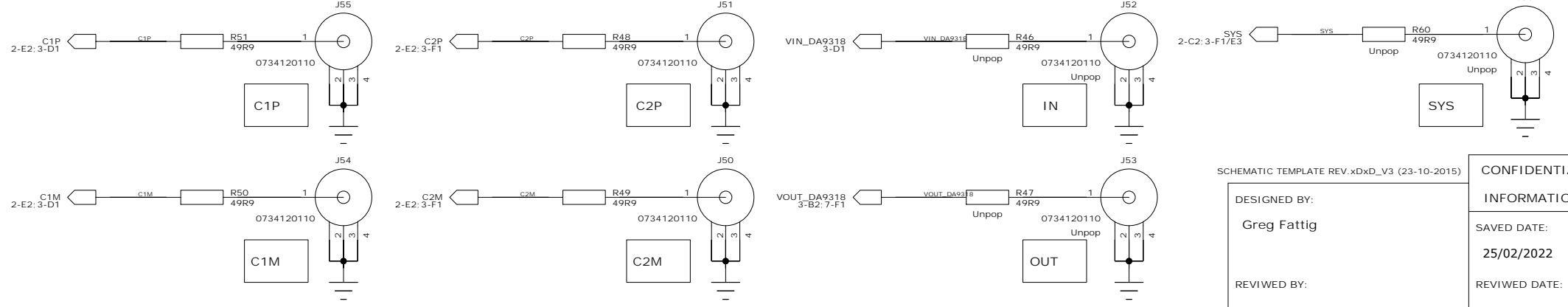
CONFIDENTIAL	SIZE A3L	TITLE: DA9318 EVB Solder
INFORMATION	SAVED DATE: 25/02/2022	DRAWING NO: 329-01-A
	REVIWED DATE: 27/09/2016	REV: AO1
SHEET NAME: POWER_AND_IOs		PAGE: 2 of 7



CHARGE PUMP



RF connectors should kelvin connect to corresponding pin on U1



SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

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REVIWED BY:
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CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 EVB Solder		
	SAVED DATE: 25/02/2022	DRAWING NO: 329-01-A	REV: A01	
REVIWED DATE: 27/09/2016	SHEET NAME: CP		PAGE: 3	of 7

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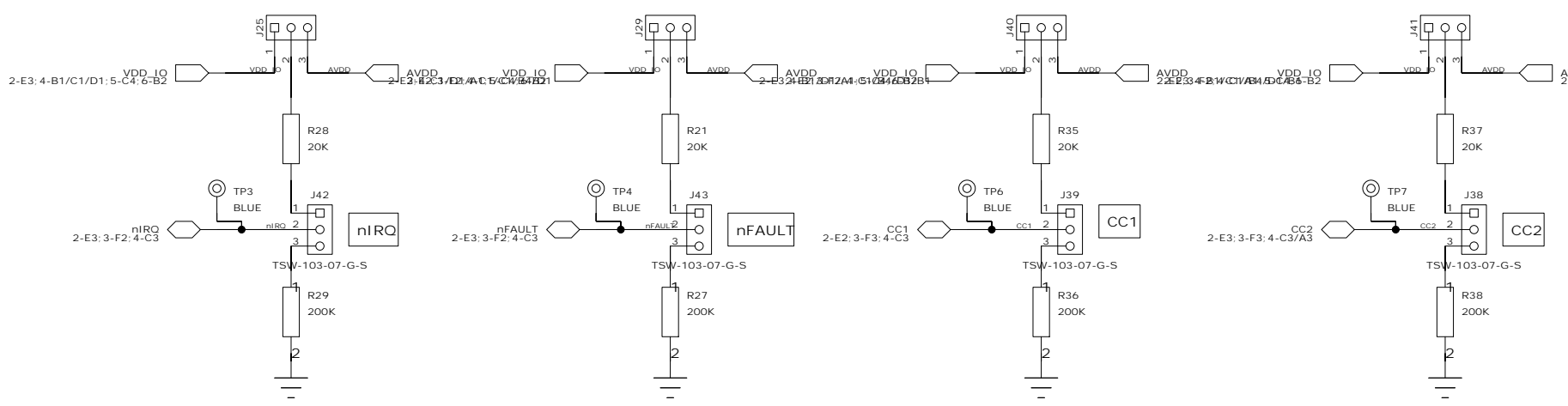
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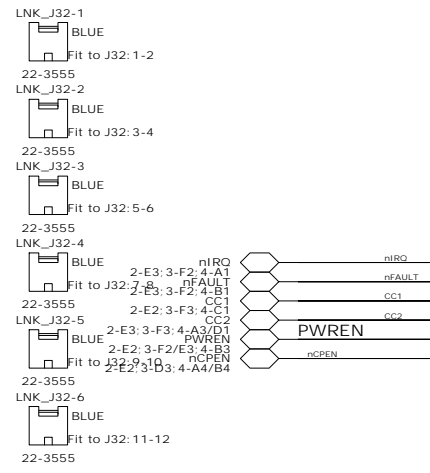
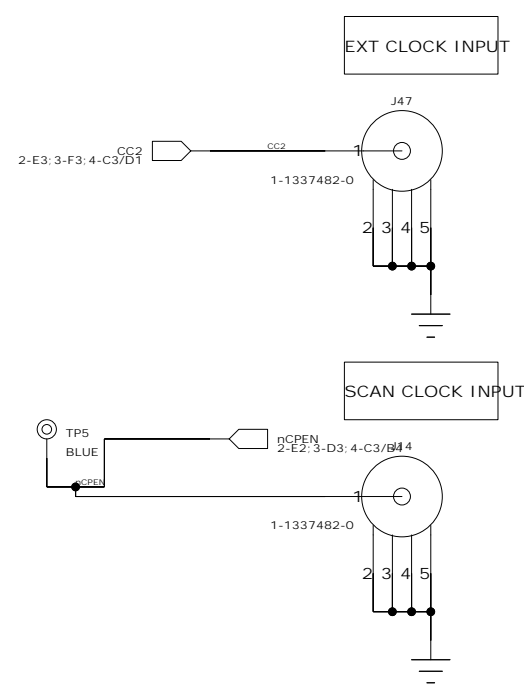
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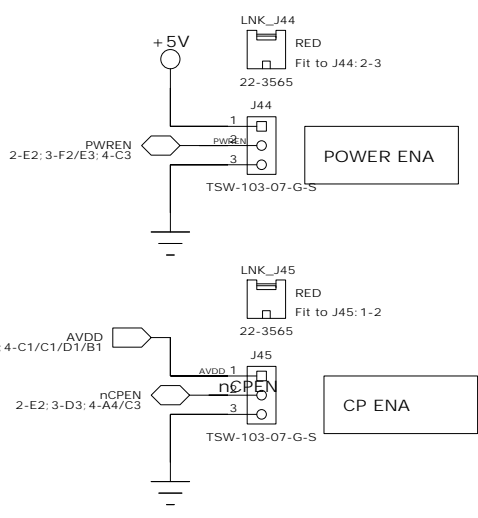
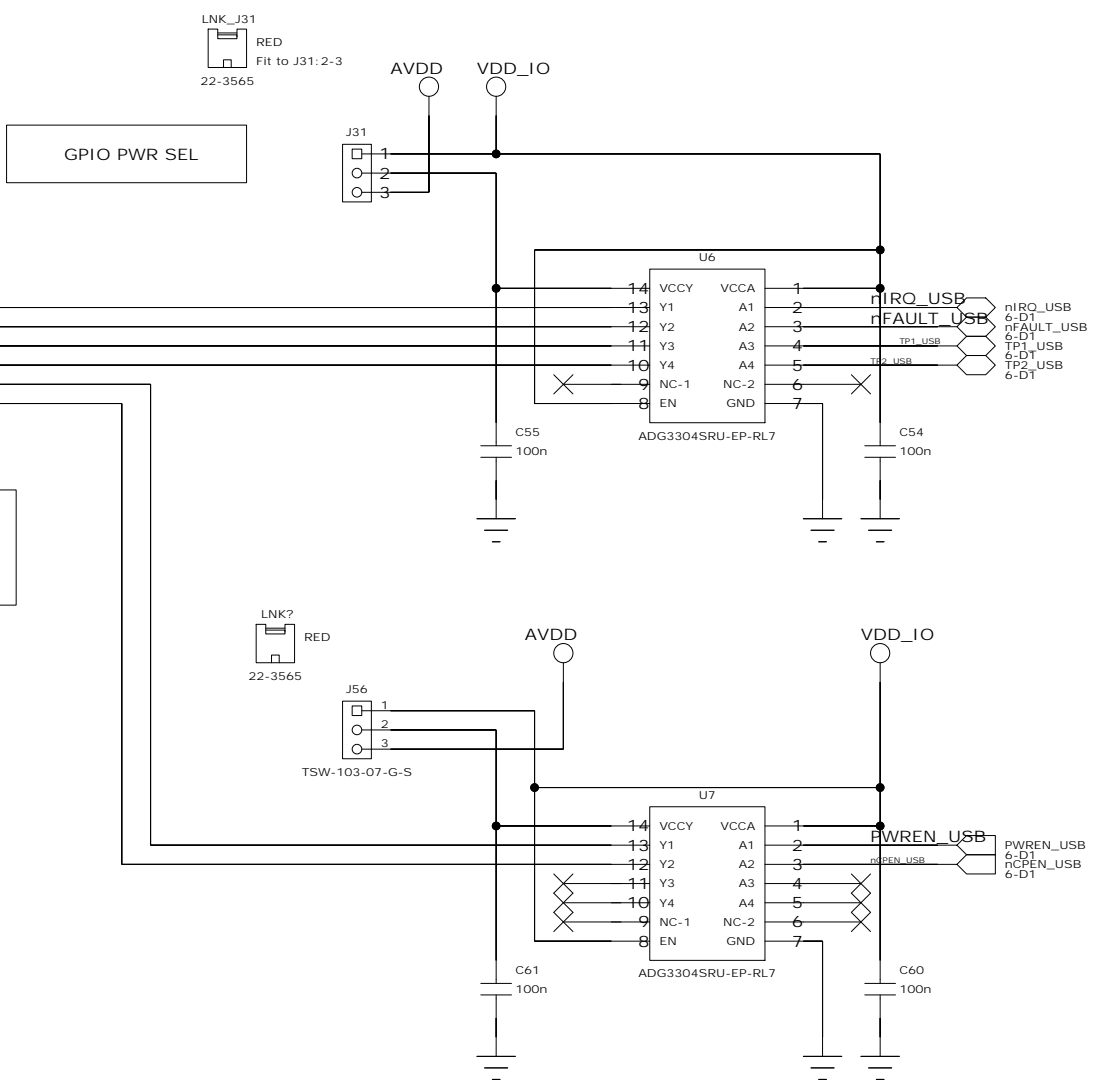


J25, J29, J40, J41	PU PWR SEL
1-2	VDD IO
2-3	AVDD

J38, J39, J42, J43	PU or PD select
1-2	Pull Up
2-3	Pull Down



SIGNALS:
nIRO
nFAULT
CC1
CC2
PWREN
nCPEN



GPIOs

SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

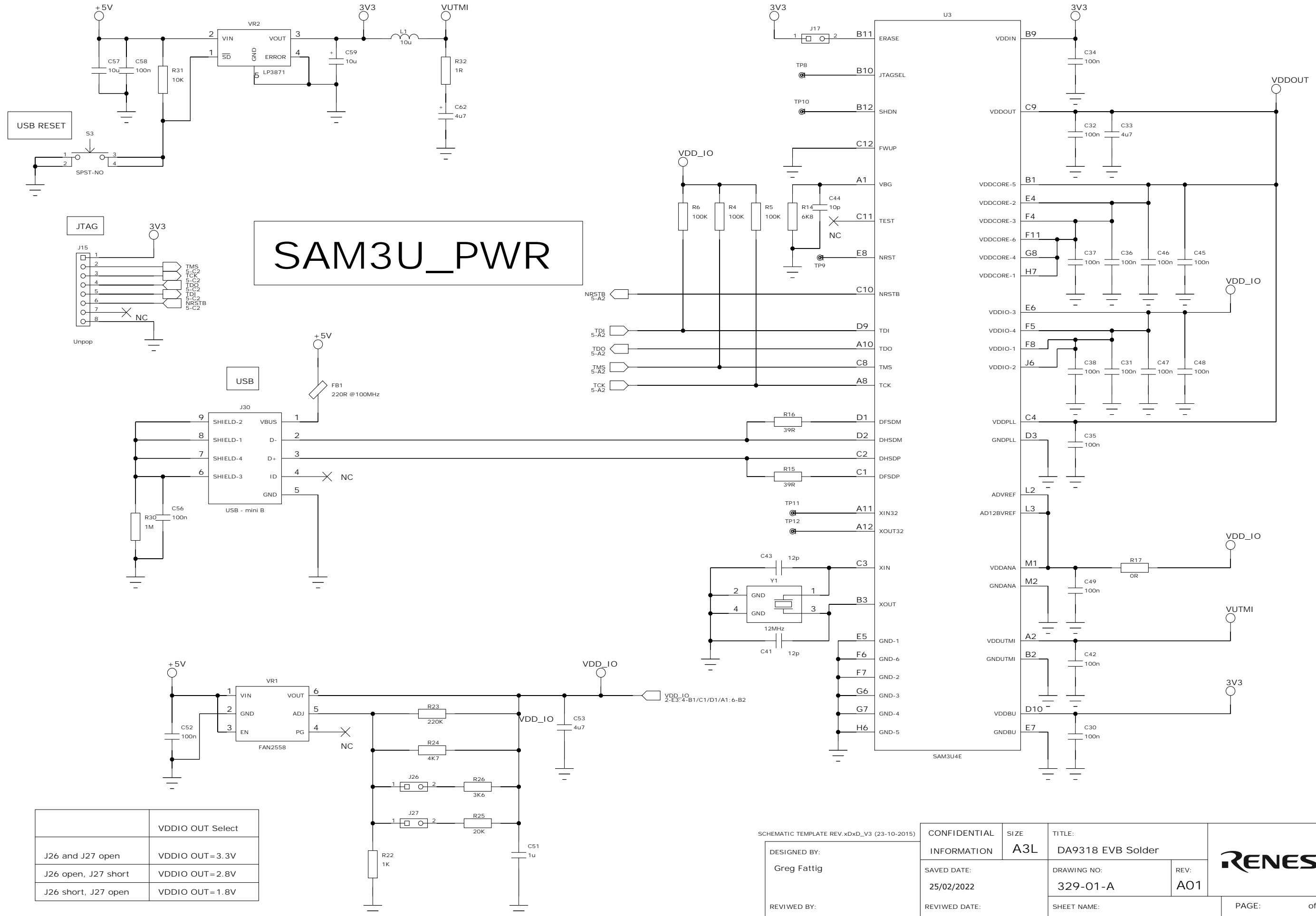
DESIGNED BY:
Greg Fattig

REVIWED BY:
GF, GC

CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 EVB Solder
SAVED DATE: 25/02/2022	DRAWING NO: 329-01-A	REV: A01
REVIWED DATE: 27/09/2016	SHEET NAME: GPIOs	



SAM3U_PWR



	VDDIO OUT Select
J26 and J27 open	VDDIO OUT=3.3V
J26 open, J27 short	VDDIO OUT=2.8V
J26 short, J27 open	VDDIO OUT=1.8V

SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

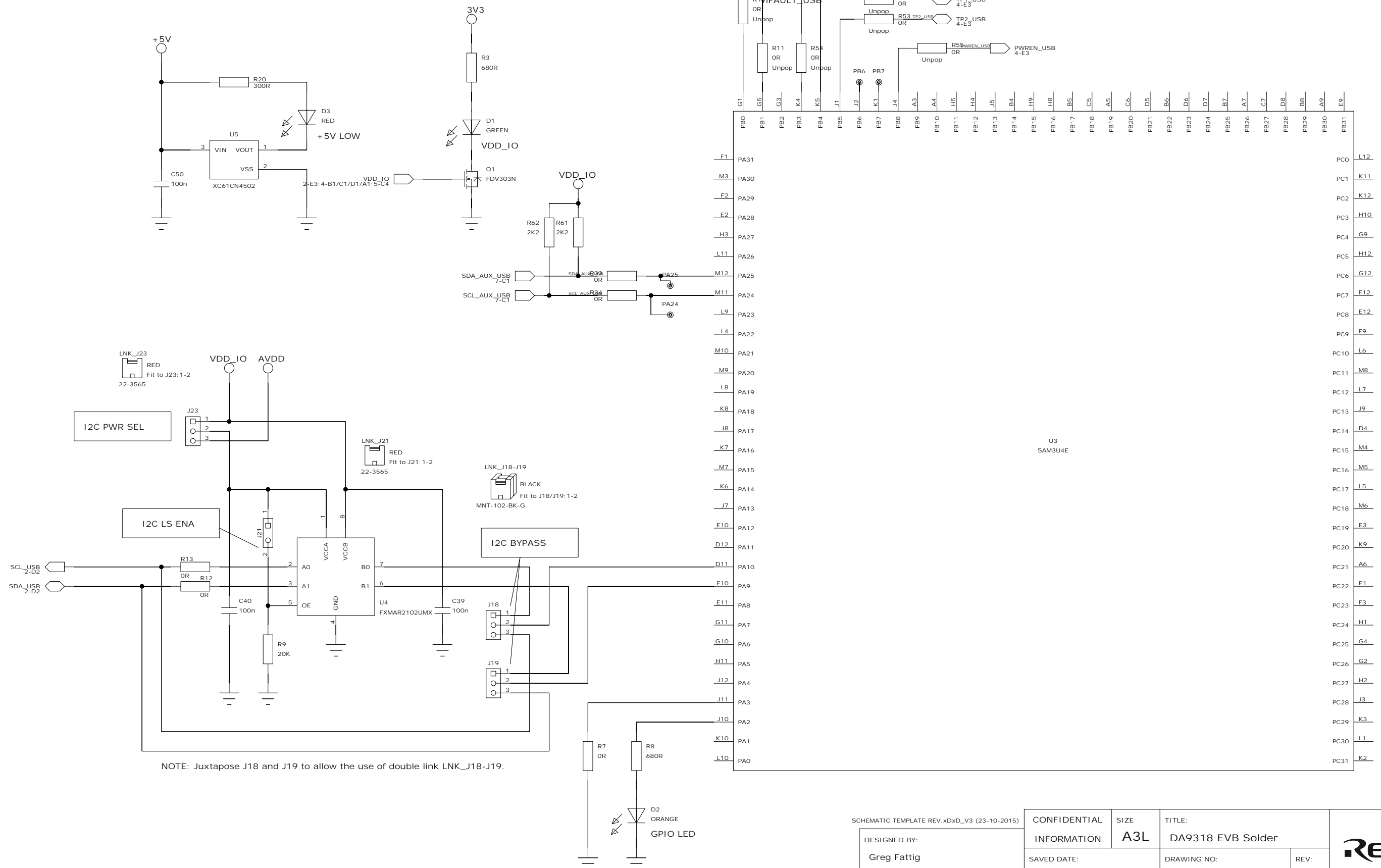
DESIGNED BY:
Greg Fattig

REVIWED BY:
GF, GC

CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 EVB Solder	REV: A01
SAVED DATE: 25/02/2022		DRAWING NO: 329-01-A	
REVIWED DATE: 27/09/2016		SHEET NAME: USB_IF	PAGE: 5 of 7



SAM3U_IOs



SCHEMATIC TEMPLATE REV. xDxD_V3 (23-10-2015)

DESIGNED BY:
Greg Fattig

REVIWED BY:
GF, GC

CONFIDENTIAL INFORMATION	SIZE A3L	TITLE: DA9318 EVB Solder	
SAVED DATE: 25/02/2022	DRAWING NO: 329-01-A	REV: A01	
REVIWED DATE: 27/09/2016	SHEET NAME: USB_LEVEL_SHIFTER	PAGE: 6 of 7	



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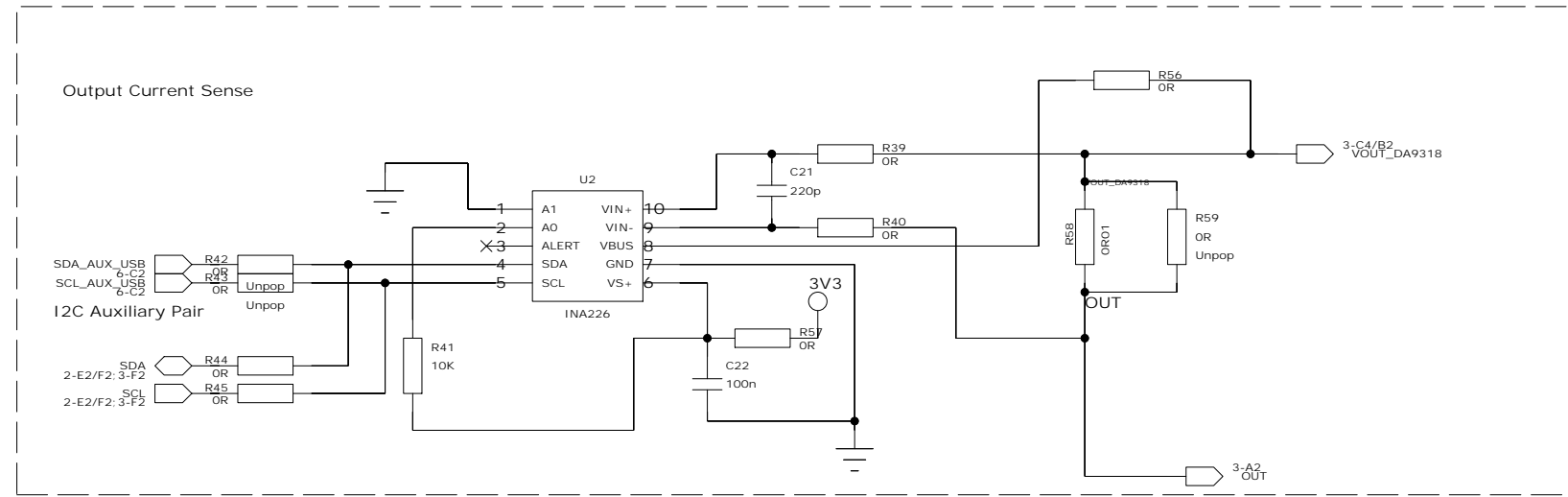
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SCHEMATIC TEMPLATE REV.xDxD_V3 (23-10-2015)

DESIGNED BY:
Greg Fattig

REVIWED BY:
GF, GC

CONFIDENTIAL
INFORMATION

SIZE
A3L

TITLE:
DA9318 EVB Solder

SAVED DATE:
25/02/2022

REVIWED DATE:
27/09/2016

DRAWING NO:
329-01-A

SHEET NAME:
ISENSE

REV:
A01

RENESAS

PAGE: 7 of 7

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