

ISL95857C

1+2+1 Voltage Regulator With Expanded Iccmax Register Range Supporting Intel IMVP8 CFL/CNL CPUs

FN8968
Rev.0.00
Oct 5, 2017

The [ISL95857C](#) provides a complete power solution for Intel microprocessors supporting core, graphics, and system agent rails and is compliant with Intel IMVP8. The controller provides control and protection for three Voltage Regulator (VR) outputs. The VR A and VR C outputs support 1-phase operation only, while VR B is configurable for 2- or 1-phase operation. The address options programmable for these three outputs allow for maximum flexibility in support of the IMVP8 CPU. All three VRs share a common serial control bus to communicate with the CPU and achieve lower cost and smaller board area compared with a two-chip approach.

Based on Intersil's Robust Ripple Regulator (R3™) technology, the R3 modulator has many advantages compared to traditional modulators. These include faster transient settling time, variable switching frequency in response to load transients, and improved light-load efficiency due to diode emulation (DE) mode with load-dependent low switching frequency.

The controller provides PWM outputs, which support Intel DrMOS power stages (or similar) and discrete power stages using the Intersil ISL95808 high voltage synchronous rectified buck MOSFET driver. The controller complies with IMVP8 PS4 power requirements and supports compatible power stages and drivers. The ISL95857C supports the system input power monitor (PSYS) option. The controller supports either DCR current sensing with a single NTC thermistor for DCR temperature compensation, or more precision through resistor current sensing if desired. All three outputs feature remote voltage sense, programmable I_{MAX} , adjustable switching frequency, OC protection, and a single VR_READY power-good indicator.

Features

- Supports the Intel serial data bus interface
 - Fully supports PS4 Power Domain entry/exit
- Supports system input power monitor (PSYS)
- Three output controller
 - VR A supports 1-phase VR design
 - VR B configurable for 2- or 1-phase VR design
 - VR C supports 1-phase VR design
- 0.5% system accuracy over temperature
- Low supply current in PS4 state
- Supports multiple current sensing methods
 - Lossless inductor DCR current sensing
 - Precision resistor current sensing
- Differential remote voltage sensing
- Programmable SVID address
- Resistor programmable address selection, I_{MAX} , and switching frequency

Applications

- IMVP8 CFL and CNL compliant notebooks, desktops, Ultrabooks, and tablets

Related Literature

- For a full list of related documents, visit our website
 - [ISL95857C](#) product page

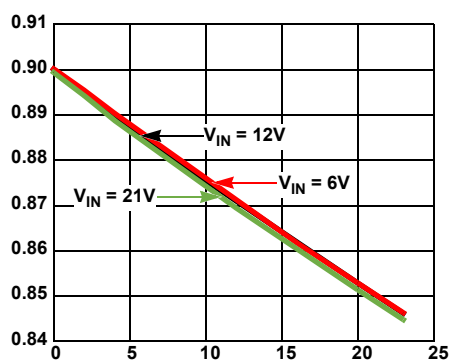


Figure 1. V_{CORE}/VR A Load Line = 2.4mΩ

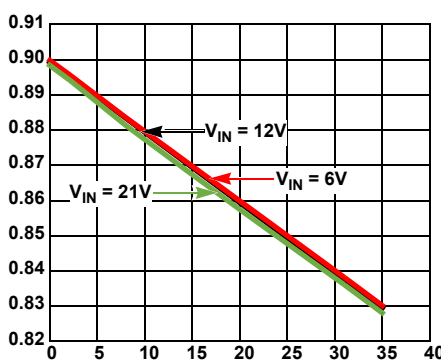


Figure 2. VGT/VR B Load Line = 2mΩ

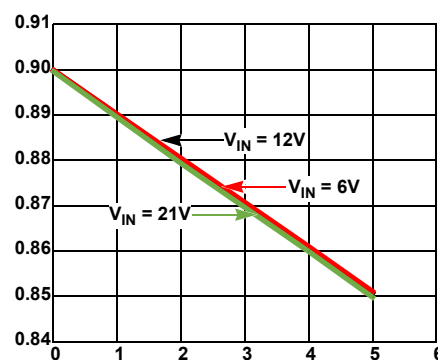


Figure 3. VSA/VR C Load Line = 10.3mΩ

**© Copyright Intersil Americas LLC 2017. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.**

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted
in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com