SC14441A/B/C, SC14442A

1.8 Single Chips for DECT with RFPA and QSPI

This short datasheet is an addendum to the SC14441A/B/C, SC14442A datasheet.

The SC14441A/B/C, SC14442A are a family of digital CMOS ICs with fully integrated radio transceivers including RF Power Amplifier and baseband processors for DECT and DECT 6.0 CAT-iQ handsets and base stations. The program memory and data storage resided in a low cost, low pin count Quad SPI (QSPI) Serial Flash. The dual row LGA approach provides a backward compatible pinning to the SC14481 devices.

Key Features

- Complies with DECT ETS 300 175-2,3 & 8 and DECT 6.0
- 10.368/20.736 MHz XTAL digital controlled oscillator
- Processing power
  - 82.944 MHz 16 bit CompactRISCTM CR16Cplus with 16 kB instruction and data cache
  - Four channel DMA controller with (non-)blocking mode
  - 82.944 MHz programmable Gen2DSP with MicroCode ROM and 2 kB MicroCode RAM
  - Dedicated Instruction Processor (DIP) supporting CAT-iQ slot formats (1.25 kB DIP RAM)
- Development/Debug support
  - Serial Debug interface, Nexus Class-1 compliant
  - Performance Timer for Gen2DSP and CR16C
  - Instruction/Data/Event Trace unit
  - Gen2DSP debugger with 2 ch. MCROM patching
- Memories
  - 16 kB + 4 kB non-shared/cache RAM
  - 32 kB shared RAM (0/1 wait cycles)
  - 48/2 kB Gen2DSP ROM/RAM
- Power management
  - 1.9 V to 3.45 V operating range
  - 1.8 V operating voltage with 1.8 V to 3.45 V I/O
  - Charge control for 2x NiMH batteries and Li-Ion
  - Dual output Voltage tripler
  - DC-DC converter with boost, buck, boost-buck operation
  - Three matched current sources for white LEDs
  - Ultra-low power mode (ULP) 32 kHz time base and low power CR16 Mode in off mode
  - Enhanced new battery detection
  - Battery voltage comparator with interrupt
- Analog and Audio Interfaces
  - Dual 8, 16, 32 kHz 16-bit linear audio CODEC
  - Analog Front End to differential and single ended microphones and 28 Ω loudspeaker
  - CLASS-D amplifier 0.5 W 2.5 V (4 Ω)
  - 10 bit ADC for line interface, Battery voltage, temperature sensor, headset detection
  - Opamps for caller-id, ringing, parallel set detection
- Digital interfaces
  - 82.944 MHz,1.8 V to 3.3 V Quad SPI interface for serial FLASH with erase suspend/resume support for EEPROM function and CAT-iQ SUOTA
  - 4+2 general purpose I/O 8 bit ports
  - Keyboard interface with debounce counter
  - Dual UART Full duplex 9600 Bd to 230.4 kBd
  - Dual SPI+™ interface 20.736 MHz (Master/Slave)
  - Dual ACCESS bus 100 kHz, 400 kHz, 1.152 MHz
  - 6 channel PCM+ Interface M/S (I2S compatible)
- Three general purpose timers and watch dog timer
- Radio transceiver
  - Integrated 1.9 GHz/1.7 GHz CMOS transceiver <70 µs RF PLL lock time
  - Four digital output ports (including two for fast antenna diversity switching)
  - -96 dBm receiver sensitivity
- Integrated 1.9 GHz PA for DECT
  - High Power Mode EU (HPM): 25.5 dBm
  - High Power Mode USA (HPM): 23.5 dBm
  - Low Power Mode (LPM): 12 dBm
  - "Green" Mode (GPM): 4 dBm
  - Low Radiation Mode (LRM): -35 dBm
  - Output power ramp and flatness control
- LGA96, LGA132 and QFN88 packages

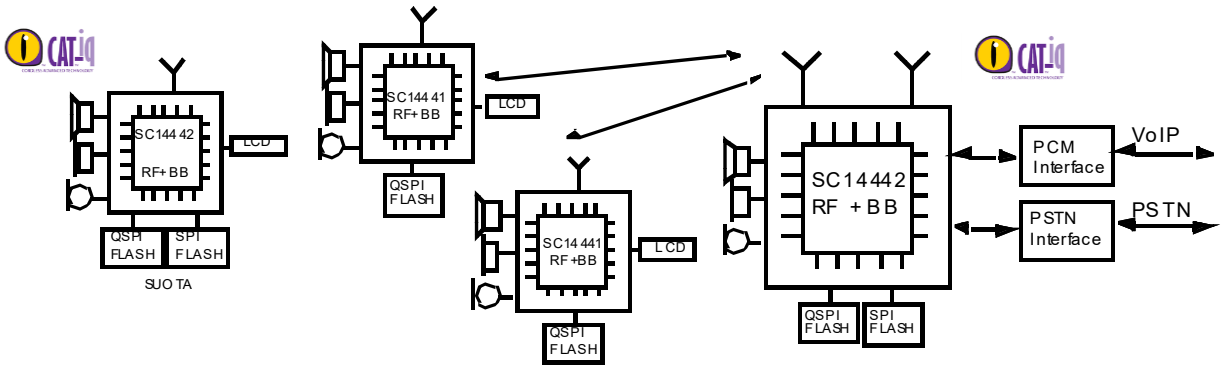

Figure 1. System diagram

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1. Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH. before the solder reflow process.

The LGA packages are qualified for MSL 3.

The QFN packages have MSL 3.

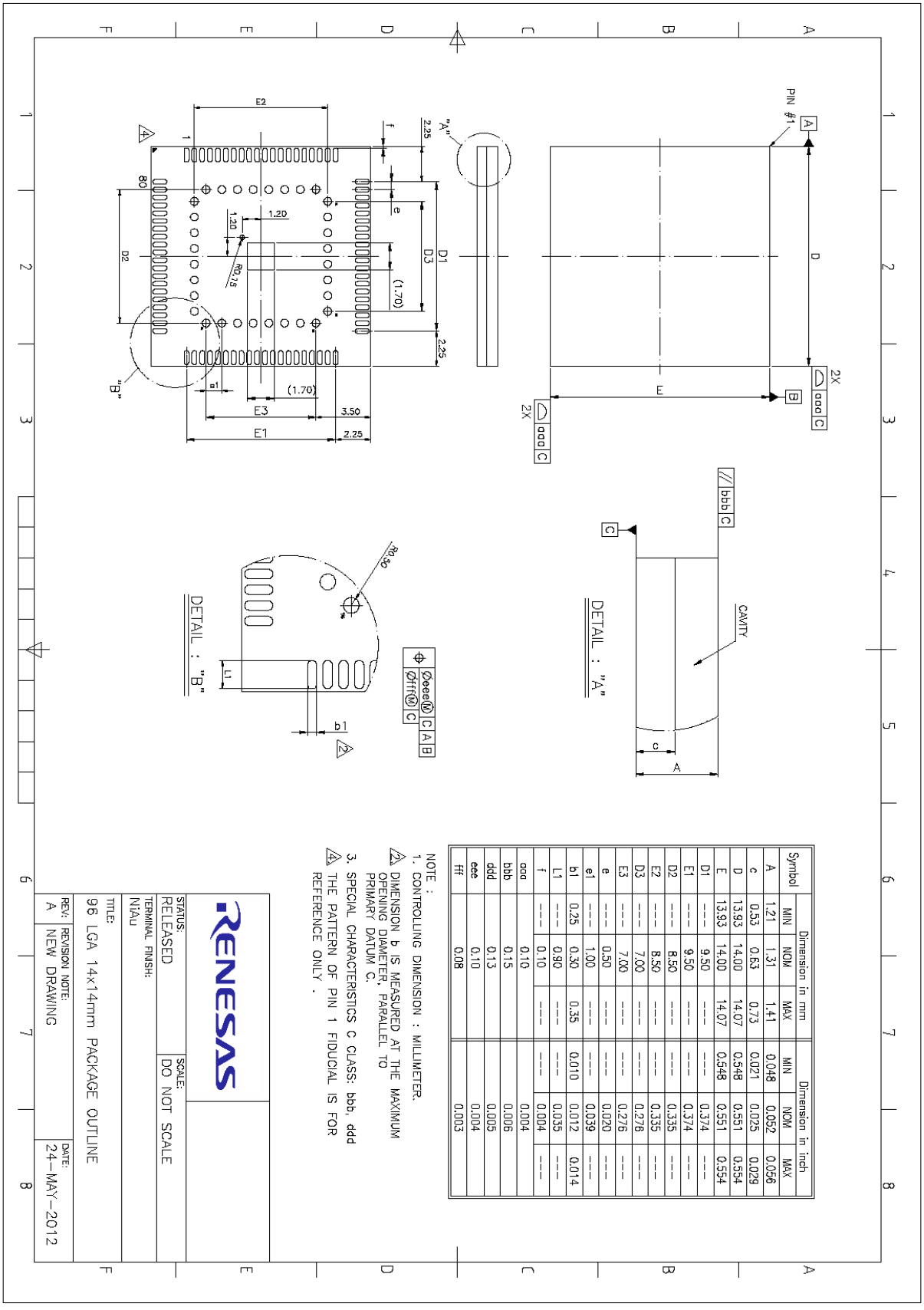
Table 1. MSL classification

MSL level	Floor lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C / 85% RH

1.1 Soldering Information

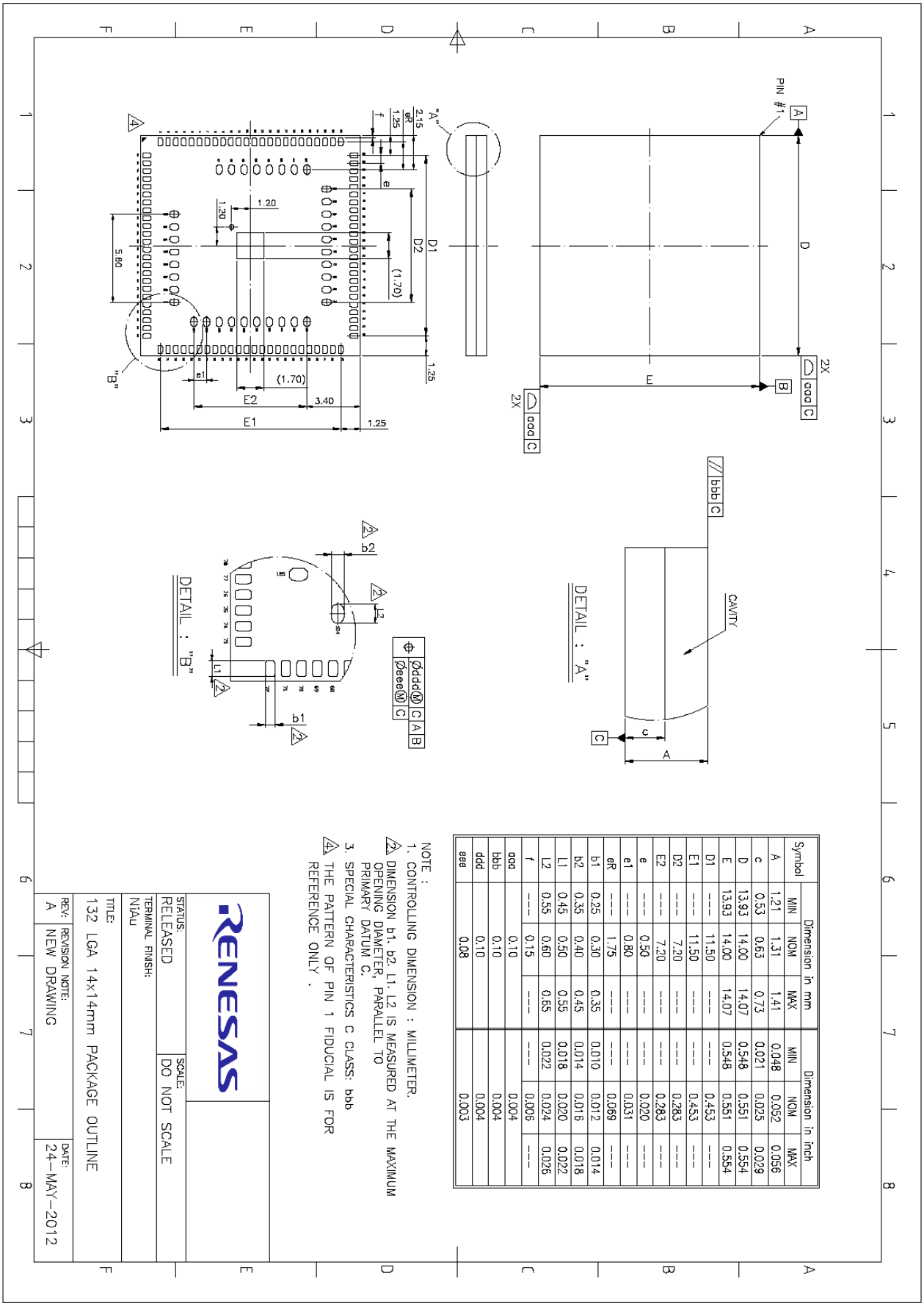
Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

2. Package Outline Drawings



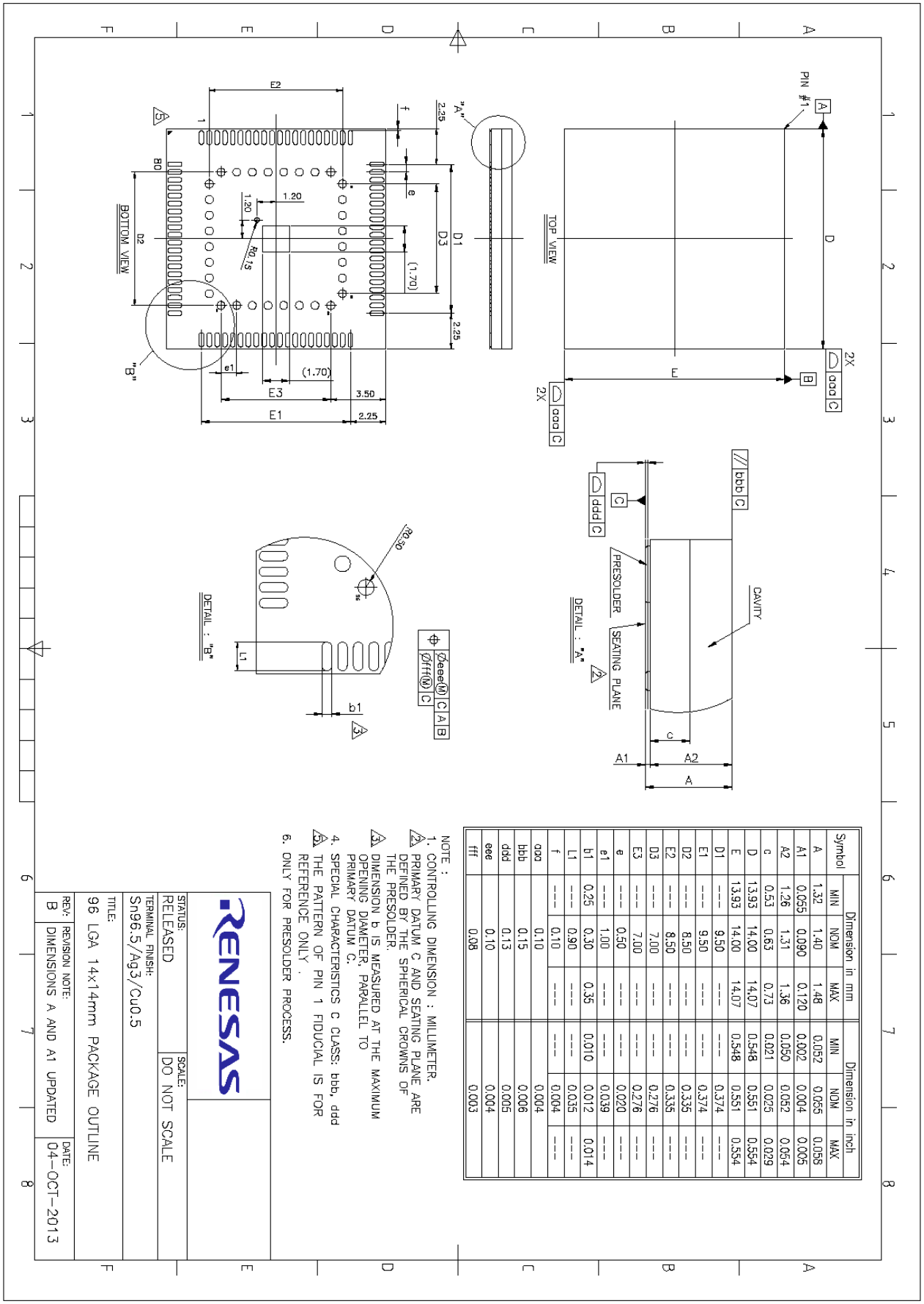
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.21	1.31	1.41	0.048	0.052	0.056
c	0.53	0.63	0.73	0.021	0.025	0.029
D	13.93	14.00	14.07	0.548	0.551	0.554
E	13.93	14.00	14.07	0.548	0.551	0.554
D1	---	9.50	---	---	0.374	---
E1	---	9.50	---	---	0.374	---
D2	---	8.50	---	---	0.335	---
E2	---	8.50	---	---	0.335	---
D3	---	7.00	---	---	0.276	---
E3	---	7.00	---	---	0.276	---
e	---	0.50	---	---	0.020	---
e1	---	1.00	---	---	0.039	---
b1	0.25	0.30	0.35	0.010	0.012	0.014
L1	---	0.90	---	---	0.035	---
f	---	0.10	---	---	0.004	---
aaa		0.10			0.004	
bbb		0.15			0.006	
ddd		0.13			0.005	
eee		0.10			0.004	
fff		0.08			0.003	

Figure 2. LGA96 package outline drawing (non-presoldered)



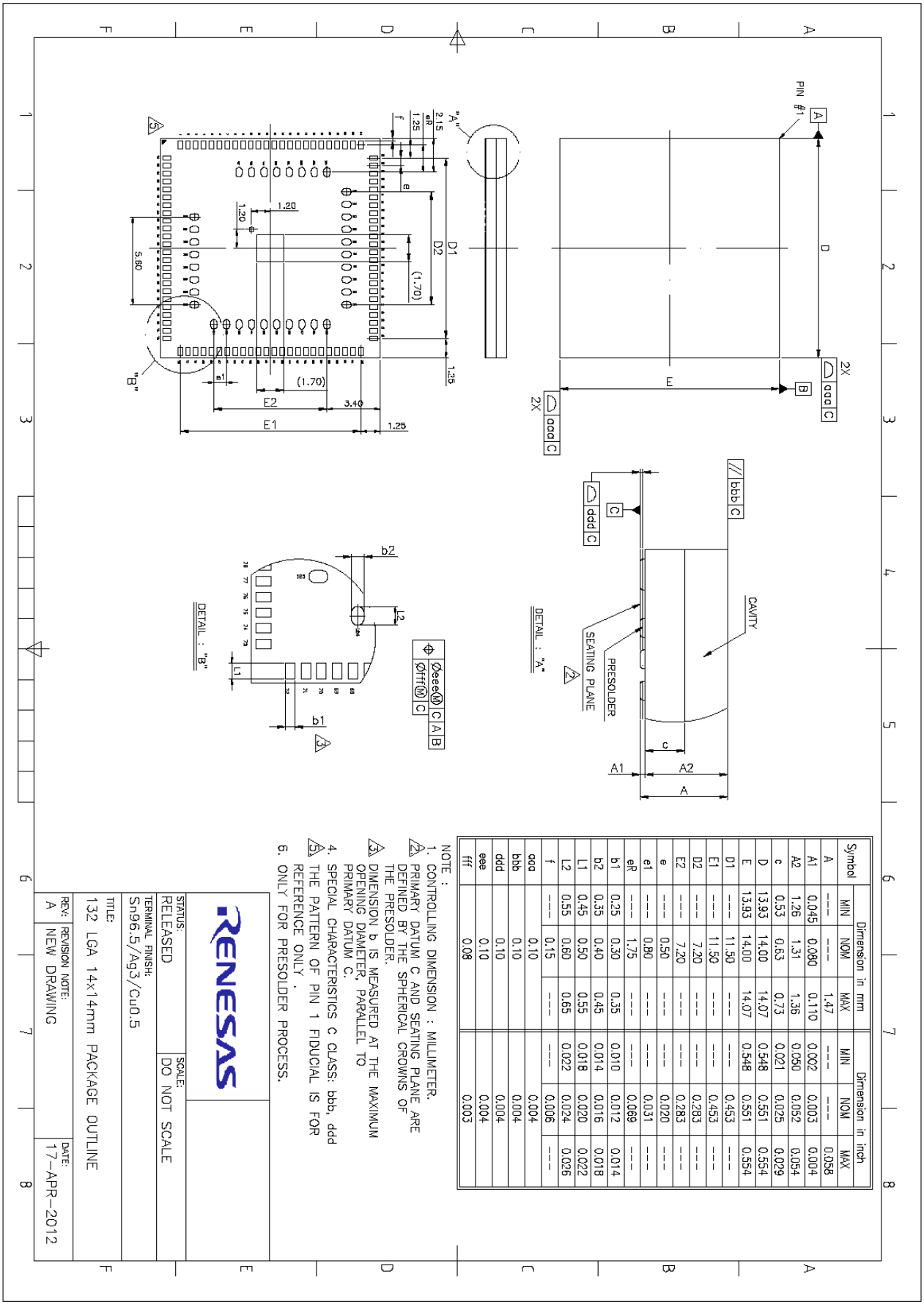
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.21	1.31	1.41	0.048	0.052	0.056
c	0.53	0.63	0.73	0.021	0.025	0.029
D	13.93	14.00	14.07	0.548	0.551	0.554
E	13.93	14.00	14.07	0.548	0.551	0.554
D1	---	11.50	---	---	0.453	---
E1	---	11.50	---	---	0.453	---
D2	---	7.20	---	---	0.283	---
E2	---	7.20	---	---	0.283	---
e	---	0.50	---	---	0.020	---
e1	---	0.80	---	---	0.031	---
eR	---	1.75	---	---	0.069	---
b1	0.25	0.30	0.35	0.010	0.012	0.014
b2	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.55	0.60	0.65	0.022	0.024	0.026
f	---	0.15	---	0.006	---	---
aaa		0.10		0.004		
bbb		0.10		0.004		
ddd		0.10		0.004		
eee		0.08		0.003		

Figure 3. LGA132 package outline drawing (non-presoldered)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.32	1.40	1.48	0.052	0.055	0.058
A1	0.055	0.090	0.120	0.002	0.004	0.005
A2	1.26	1.31	1.36	0.050	0.052	0.054
c	0.53	0.63	0.73	0.021	0.025	0.029
D	13.93	14.00	14.07	0.548	0.551	0.554
E	13.93	14.00	14.07	0.548	0.551	0.554
D1	---	9.50	---	---	0.374	---
E1	---	9.50	---	---	0.374	---
D2	---	8.50	---	---	0.335	---
E2	---	8.50	---	---	0.335	---
D3	---	7.00	---	---	0.276	---
E3	---	7.00	---	---	0.276	---
e	---	0.50	---	---	0.020	---
e1	---	1.00	---	---	0.039	---
b1	0.25	0.30	0.35	0.010	0.012	0.014
L1	---	0.90	---	---	0.035	---
f	---	0.10	---	---	0.004	---
aaa		0.10			0.004	
bbb		0.15			0.006	
ddd		0.13			0.005	
eee		0.10			0.004	
fff		0.08			0.003	

Figure 4. LGA96 package outline drawing (presoldered)



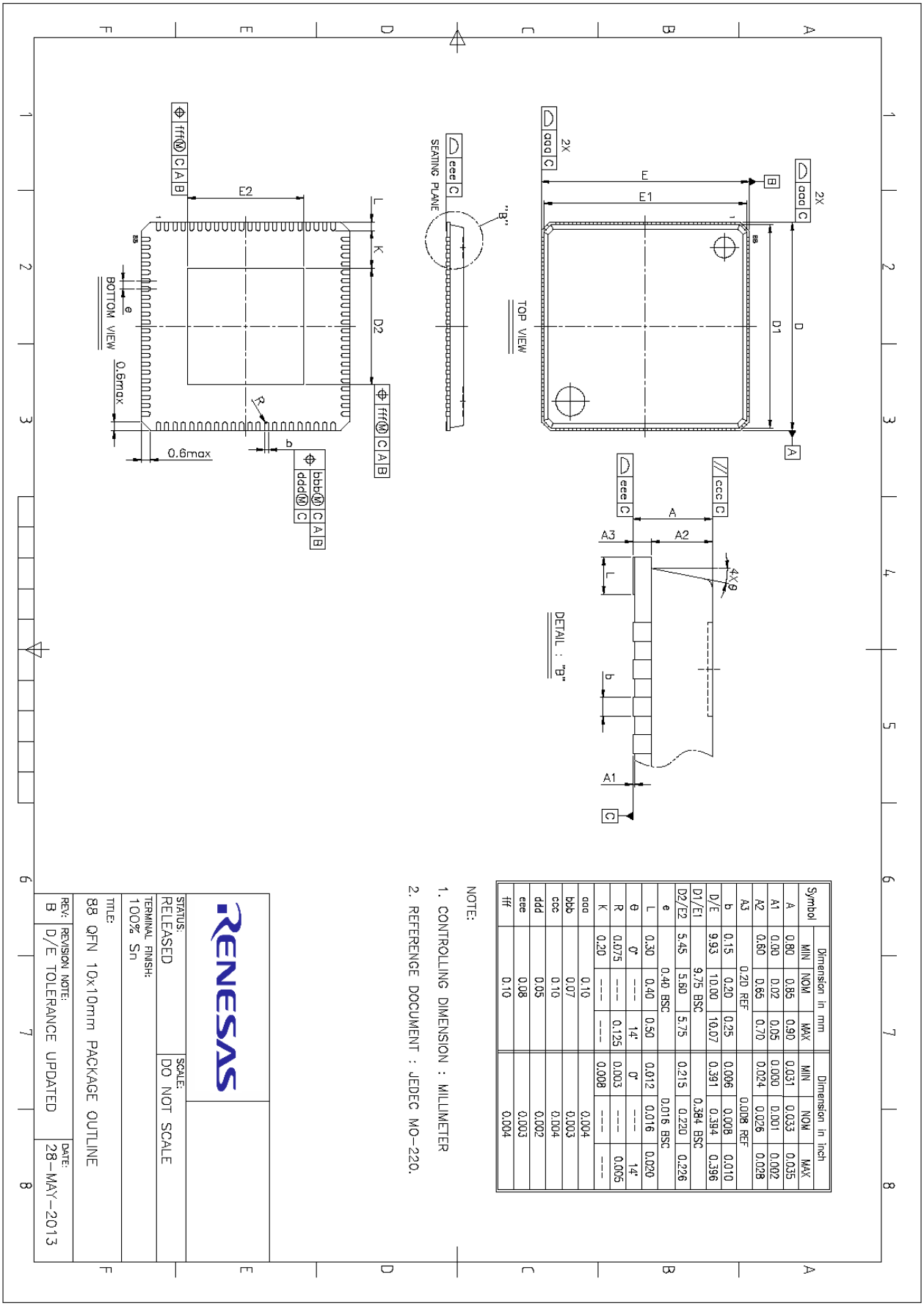
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.47	---	---	0.058
A1	0.045	0.080	0.110	0.002	0.003	0.004
A2	1.26	1.31	1.36	0.050	0.052	0.054
c	0.53	0.63	0.73	0.021	0.025	0.029
D	13.93	14.00	14.07	0.548	0.551	0.554
E	13.93	14.00	14.07	0.548	0.551	0.554
D1	---	11.50	---	---	0.453	---
E1	---	11.50	---	---	0.453	---
D2	---	7.20	---	---	0.283	---
E2	---	7.20	---	---	0.283	---
e	---	0.50	---	---	0.020	---
e1	---	0.80	---	---	0.031	---
eR	---	1.75	---	---	0.069	---
b1	0.25	0.30	0.35	0.010	0.012	0.014
b2	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.55	0.60	0.65	0.022	0.024	0.026
f	---	0.15	---	---	0.006	---
aaa		0.10			0.004	
bbb		0.10			0.004	
ddd		0.10			0.004	
eee		0.10			0.004	
fff		0.08			0.003	

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE PRESOLDER.
3. DIMENSION b IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. ONLY FOR PRESOLDER PROCESS.

RENESAS

STATUS: RELEASED
SCALE: DO NOT SCALE
TERMINAL FINISH: Sn96.5/Ag3/Cu0.5
TITLE: 132 LGA 14x14mm PACKAGE OUTLINE
REV: A
REVISION NOTE: NEW DRAWING
DATE: 17-APR-2012

Figure 5. LGA132 package outline drawing (presoldered)



Symbol	Dimension in mm				Dimension in inch			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	0.80	0.85	0.90		0.031	0.033	0.035	
A1	0.00	0.02	0.05		0.000	0.001	0.002	
A2	0.60	0.65	0.70		0.024	0.026	0.028	
A3		0.20 REF				0.008 REF		
b	0.15	0.20	0.25		0.006	0.008	0.010	
D/E	9.93	10.00	10.07		0.391	0.394	0.396	
D1/E1		9.75 BSC				0.384 BSC		
D2/E2	5.45	5.60	5.75		0.215	0.220	0.226	
e		0.40 BSC				0.016 BSC		
L	0.30	0.40	0.50		0.012	0.016	0.020	
θ	0°	---	14°		0°	---	14°	
R	0.075	---	0.125		0.003	---	0.005	
K	0.20	---	---		0.008	---	---	
aaa		0.10				0.004		
bbb		0.07				0.003		
ccc		0.10				0.004		
ddd		0.05				0.002		
eee		0.08				0.003		
fff		0.10				0.004		

Figure 6. QFN88 (5.6 x 5.6 mm Epad) package outline drawing

3. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 2. Ordering information

Part number	Package	Size (mm)	Shipment form	Pack quantity
SC14441C52R101QNCT	QFN88 package	10 x 10	Tray	MOQ 1680
SC14441B52RLT	LGA96 package	14 x 14	Tray	MOQ 1190

4. Revision History

Revision	Date	Description
01.00	June 26, 2024	First release.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.