Renesas Radiation Tolerant Plastic Screening and QCI Flow

This document outlines the production flow and lot assurance testing for Renesas Radiation Tolerant Plastic products for space applications. Refer to the datasheet for each device for more information specific to that device.

Contents

1. Introduction

The production and screening flow detailed in this document applies to all Renesas Radiation Tolerant Plastic products.

2. Production Flow

This section outlines the production flow that Renesas Radiation Tolerant Plastic parts receive after assembly.

After parts have been assembled, all units go through the Production Screening Procedure, detailed further in Production Screening Procedure. Starting on August 1, 2023, after the ICs pass the Production Screening Procedure, sample selection for Quality Conformance Inspection (QCI) occurs, discussed further in Quality Conformance Inspection. The remaining ICs go on quality hold pending QCI recommendation. Finally, when QCI has passed, the ICs placed on quality hold move into inventory and become orderable. If the sampled ICs fail QCI, the ICs on quality hold are scrapped and can never be ordered.

The flowcharts in this document are used as a visual representation of the production screening and QCI flow. However, the order of the tests is subject to change based on manufacturing needs.

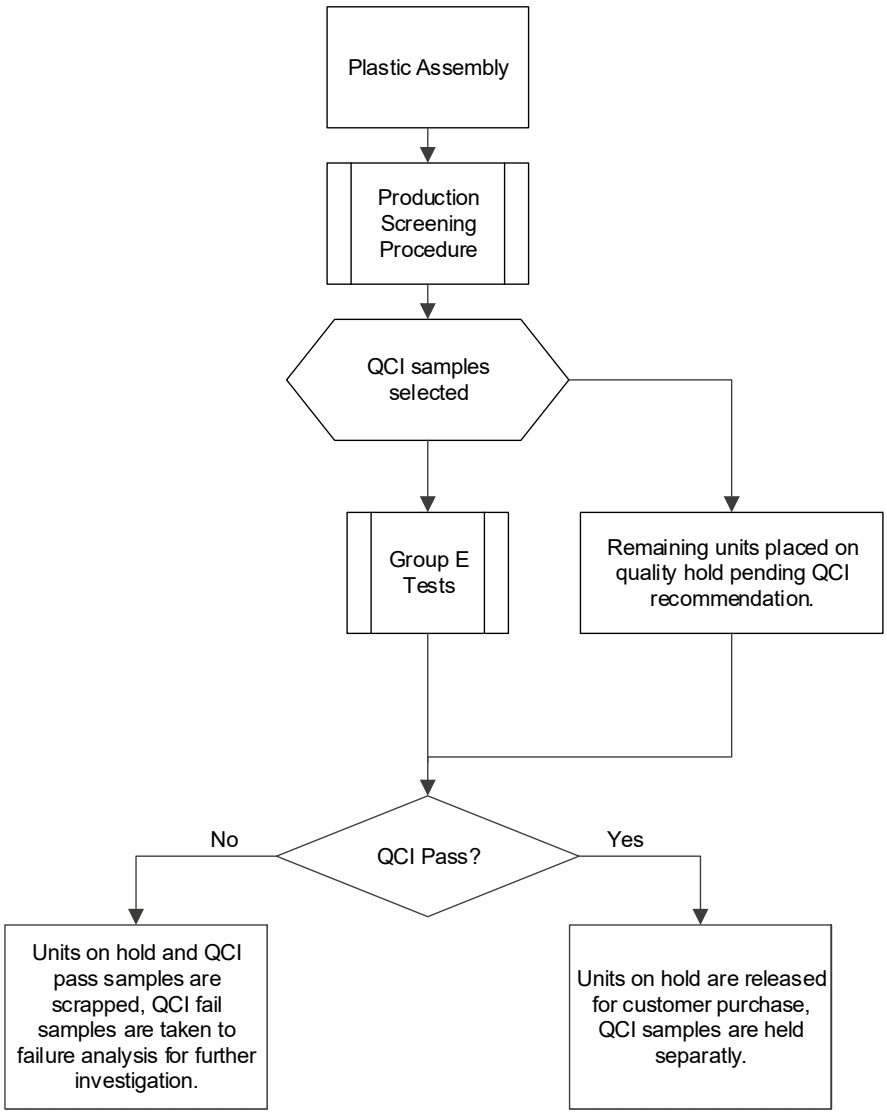

Figure 1. Radiation Tolerant Plastic Production Flow Chart

3. Production Screening Procedure

This section outlines the production screening that 100% of Renesas Radiation Tolerant Plastic units receive.

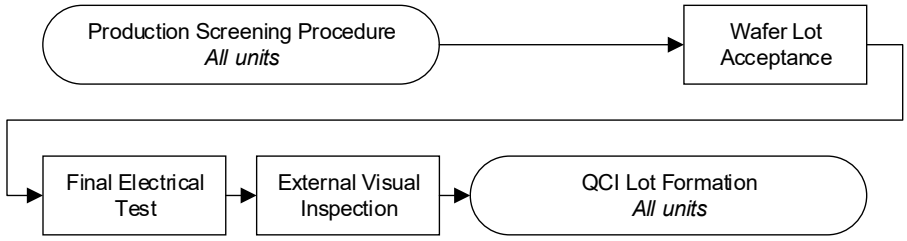

Figure 2. Production Screening Procedure Flow Chart

Table 1. Production Screening Procedure Test Method Descriptions

Test	Test Method	Notes
Wafer Lot Acceptance	MIL-STD-883 TM5007	-
Final Electrical Test	Per device specification	25°C[1]
External Visual Inspection	MIL-STD-883 TM2009	-

1. One unit further tested at minimum and maximum operating temperatures as an additional manufacturing and production check.

4. Quality Conformance Inspection

This section outlines the Quality Conformance Inspection testing that follows the production screening procedure.

After units undergo the production screening procedure outlined in Production Screening Procedure, samples are selected for Quality Conformance Inspection (QCI). The ICs not selected for QCI are held for customer purchase, pending QCI recommendation.

Table 2. QCI Sampling Quantities and Frequencies

Test	Minimum Number of Samples (Allowed Fails)	Frequency
Group E Tests (Subgroup 2)	10(0)	Every wafer lot

4.1 Group E Tests

As a part of QCI, Group E Tests (Radiation Hardness Assurance Tests) are performed, shown in Figure 3.

For Group E tests, the radiation levels a given device is qualified to can be found on its respective datasheet and radiation reports.

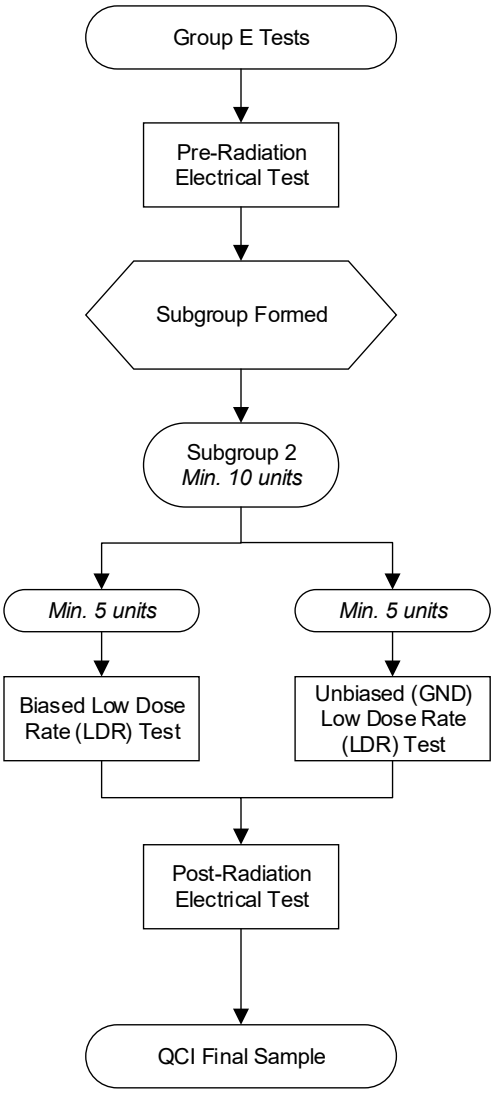

Figure 3. Group E Testing Flow Chart

Table 3. Group E Test Method Descriptions

Test	Test Method	Notes
Pre-Radiation Electrical Test	Per device specification, read and record	
Biased Low Dose Rate (LDR) Test	MIL-STD-883 TM1019	Radiation level as per device specification
Unbiased (GND) Low Dose Rate (LDR) Test	MIL-STD-883 TM1019	Radiation level as per device specification
Post-Radiation Electrical Test	Per device specification, read and record	

5. Up-Front Characterization and Qualification

This section outlines the one-time, up-front characterization and qualification that products receive. These tests are only performed during initial qualification or after any major design and/or process change. These tests are performed in addition to the standard production screening flow and quality conformance inspection. Reliability summaries are available on request for individual products.

Table 4. Up-Front Characterization Samples

Test Group	Test	Minimum Number of Samples
Package Related Tests	Moisture Resistance Testing MSL1 Test Procedure	22(0)
Package Related Tests	Moisture Resistance Testing MSL2 Test Procedure	22(0)
Package Related Tests	Moisture Resistance Testing MSL3 Test Procedure	22(0)
Package Related Tests	Biased HAST Test	80(0)
Package Related Tests	Unbiased HAST Test	80(0)
Package Related Tests	High-Temperature Storage Test	50(0)
Package Related Tests	Temperature Cycling	80(0)
Device Related Tests	Human Body Model (HBM) Electrostatic Discharge (ESD) Sensitivity Test	3(0)
Device Related Tests	Charge Device Model (CDM) Electrostatic Discharge (ESD) Sensitivity Test	3(0)
Device Related Tests	Latch-Up Test	3(0)
Device Related Tests	HTOL Test	80(0)
Radiation Related Tests	Biased Low Dose Rate (LDR) Test	5(0)
Radiation Related Tests	Unbiased (GND) Low Dose Rate (LDR) Test	5(0)
Radiation Related Tests	Destructive Single Event Effects (DSEE) Test	4(0)
Radiation Related Tests	Single Event Transient (SET) Test	4(0)

5.1 Package Related Tests

As a part of one-time, up-front characterization, specific package-related tests are performed, as shown in Figure 4.

These tests ensure the package is built reliably and no defects exist. Before these tests, a preconditioning procedure takes place, detailed further in Preconditioning Procedure.

The Moisture Sensitivity Level (MSL) is first determined through Moisture Resistance Testing to perform the correct preconditioning procedure based on the package's characteristics, detailed further in Moisture Resistance Testing. After the MSL is determined, the appropriate preconditioning procedure can occur. This preconditioning procedure occurs before every other package-related test.

For package-related tests, electrical tests are performed at 25°C and the maximum operating temperature to maximize mechanical stress after the package stress, based on AEC-Q100.

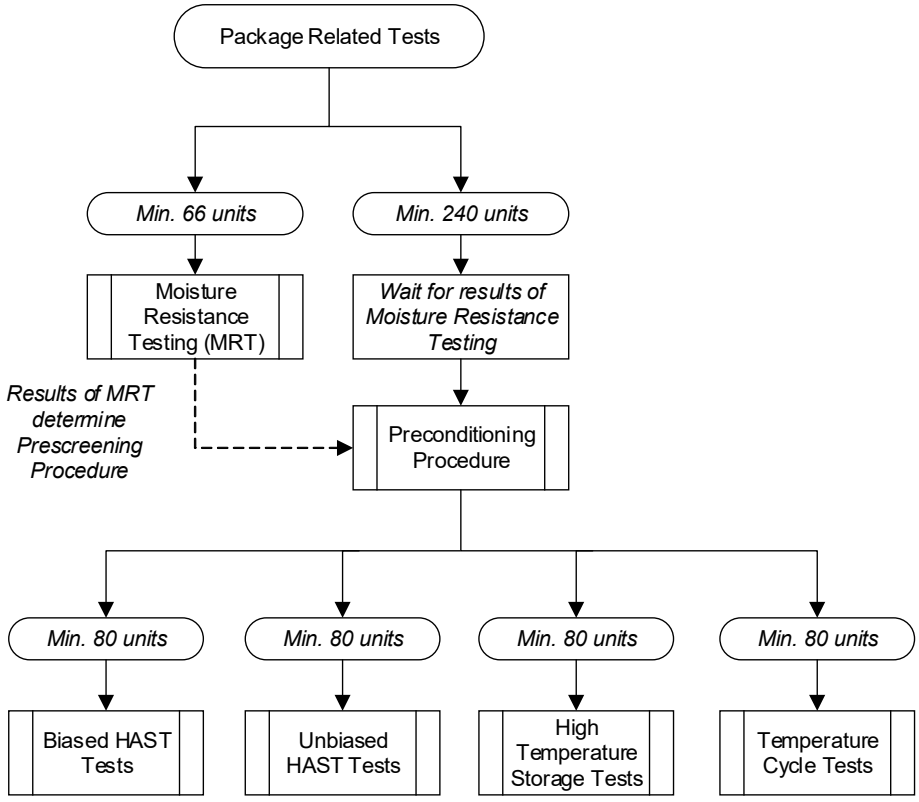

Figure 4. Package-Related Tests Flow Chart

5.1.1 Moisture Resistance Testing

The MSL is determined through Moisture Resistance Testing to determine the correct preconditioning procedure. To ensure less stringent handling requirements for end users, Renesas Radiation Tolerant Plastic ICs, at worst, have an MSL of 3.

Three parallel test flows are performed based on the three targeted MSLs (Figure 5) to determine the MSL of an IC. After these tests are complete, an engineering review of electrical test results and acoustic microscopy images takes place to assign MSL classification based on J-STD-020.

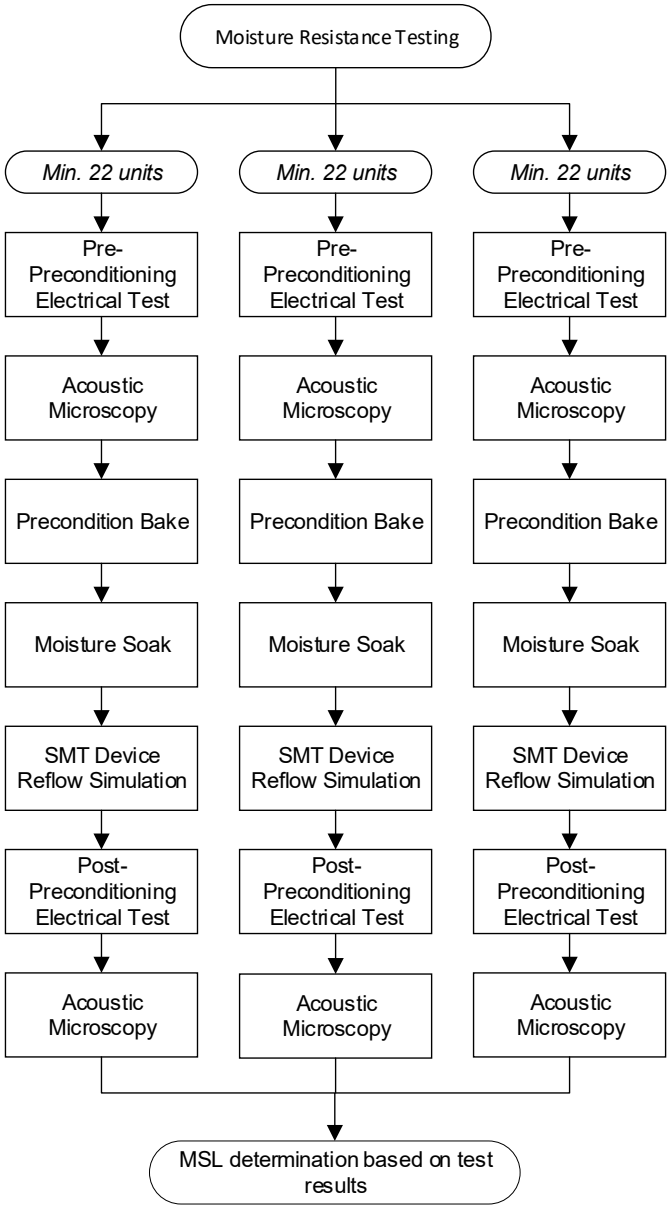

Figure 5. Moisture Resistance Testing Flow Chart

Table 5. Moisture Resistance Testing Test Methods

Test	Test Method	Notes
Pre-Preconditioning Electrical Test	Per device specification	25°C and max. operating temperature
Acoustic Microscopy	J-STD-020, J-STD-035	
Precondition Bake		125°C +5°/-0°C for 4 hours minimum
Moisture Soak: MSL 1	JESD22-A113, paragraph 4.5 per applicable moisture sensitivity level (MSL) per J-STD-020	85°C, 80% RH 168 Hours
Moisture Soak: MSL 2	JESD22-A113, paragraph 4.5 per applicable moisture sensitivity level (MSL) per J-STD-020	85°C, 60% RH 168 Hours
Moisture Soak: MSL 3	JESD22-A113, paragraph 4.5 per applicable moisture sensitivity level (MSL) per J-STD-020	30°C, 60% RH 192 Hours
SMT Device Reflow Simulation	JESD22-A113, paragraph 4.6 through 4.9	Peak solder reflow temperature +235°C
Post-Preconditioning Electrical Test	Per device specification	25°C and max. operating temperature

5.1.2 Preconditioning Procedure

All samples selected for Package-Related Tests are exposed to a preconditioning procedure. This preconditioning procedure mimics the stresses the package receives in a space environment, as shown in Figure 6.

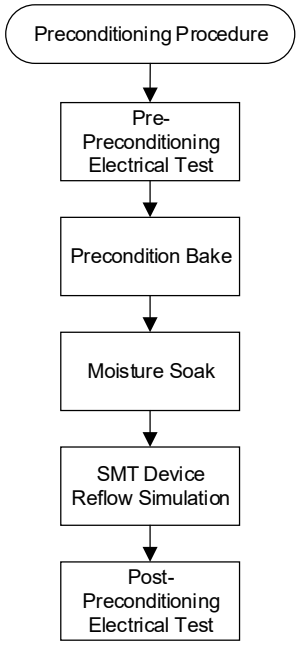

Figure 6. Preconditioning Procedure Flow Chart

Table 6. Preconditioning Procedure Test Methods

Test	Test Method	Notes
Pre-Preconditioning Electrical Test	Per device specification	25°C and max. operating temperature
Precondition Bake		125°C +5°/-0°C for 4 hours minimum

Table 6. Preconditioning Procedure Test Methods (Cont.)

Test	Test Method	Notes
Moisture Soak	JESD22-A113, paragraph 4.5 per applicable moisture sensitivity level (MSL) per J-STD-020	Conditions are dependent on MSL level, see Moisture Resistance Testing. ▪ MSL 1: 85°C, 85% RH 168 hours ▪ MSL 2: 85°C, 60% RH 168 hours ▪ MSL 3: 30°C, 60% RH 192 hours
SMT Device Reflow Simulation	JESD22-A113, paragraph 4.6 through 4.9	Peak solder reflow temperature +235°C
Post-Preconditioning Electrical Test	Per device specification	25°C and max. operating temperature

5.1.3 Biased HAST Tests

As a part of package-related tests, biased HAST tests are performed after the Preconditioning Procedure, as shown in Figure 7.

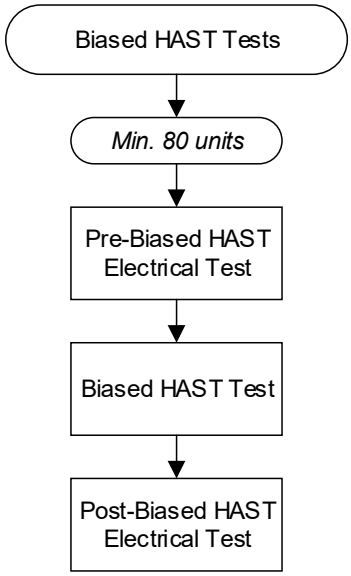

Figure 7. Biased HAST Tests Flow Chart

Table 7. Biased HAST Test Methods

Test	Test Method	Notes
Pre-Biased HAST Electrical Test	Per device specification	25°C and max. operating temperature
Biased HAST Test	JESD22-A110, with continuous bias	96 hours, +130°C, 85% RH
Post-Biased HAST Electrical Test	Per device specification	25°C and max. operating temperature

5.1.4 Unbiased HAST Tests

As a part of package-related tests, unbiased HAST test are performed after the Preconditioning Procedure, as shown in Figure 8.

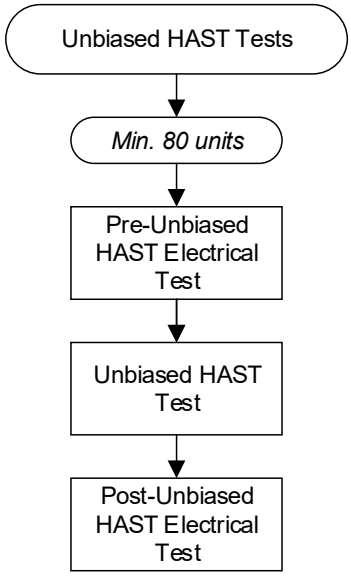

Figure 8. Unbiased HAST Tests Flow Chart

Table 8. Unbiased HAST Test Methods

Test	Test Method	Notes
Pre-Unbiased HAST Electrical Test	Per device specification	25°C and max. operating temperature
Unbiased HAST Test	JESD22-A118	130°C / 85% RH, 96hrs
Post-Unbiased HAST Electrical Test	Per device specification	25°C and max. operating temperature

5.1.5 High-Temperature Storage Tests

As a part of package-related tests, high temperature storage tests are performed after the Preconditioning Procedure, as shown in Figure 9.

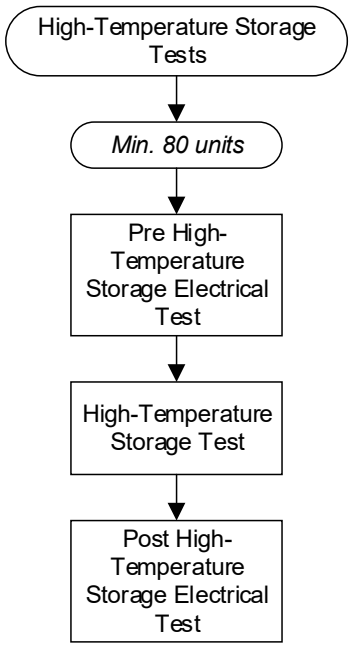

Figure 9. High-Temperature Storage Tests Flow Chart

Table 9. High-Temperature Storage Test Methods

Test	Test Method	Notes
Pre High-Temperature Storage Electrical Test	Per device specification	25°C and max. operating temperature
High-Temperature Storage Test	JESD22-A103 and A113	150°C, 1000hrs
Post High-Temperature Storage Electrical Test	Per device specification	25°C and max. operating temperature

5.1.6 Temperature Cycle Tests

As a part of package-related tests, temperature cycle tests are performed after the Preconditioning Procedure, as shown in Figure 10.

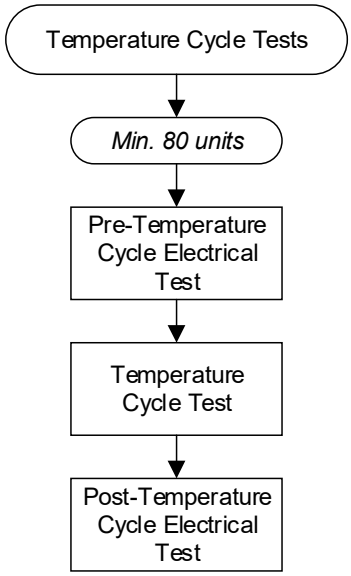

Figure 10. Temperature Cycle Tests Flow Chart

Table 10. Temperature Cycle Test Methods

Test	Test Method	Notes
Pre-Temperature Cycle Electrical Test	Per device specification	25°C and max. operating temperature
Temperature Cycle Test	MIL-STD-883 TM1010	Condition B, 65°C to 150 °C, 500 Cycles minimum
Post-Temperature Cycle Electrical Test	Per device specification	25°C and max. operating temperature

5.2 Device Related Tests

As a part of a one-time, up-front characterization, certain device-related tests are performed, as shown in Figure 11.

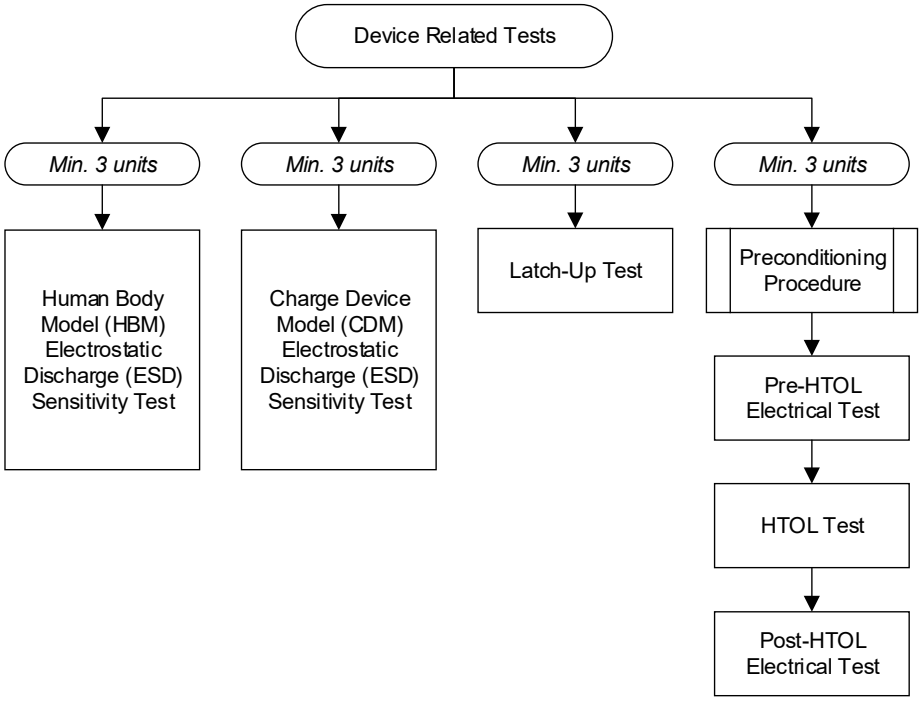

Figure 11. Up-Front Characterization Device Related Tests Flowchart

Table 11. Up-Front Characterization Device Related Test Descriptions

Test	Test Method	Notes
Human Body Model (HBM) Electrostatic Discharge (ESD) Sensitivity Test	MIL-STD-883 TM3015 or JEDEC Test Standard JS-001	Assembly and test areas use JESD625 specification controls
Charge Device Model (CDM) Electrostatic Discharge (ESD) Sensitivity Test	MIL-STD-883 TM3015 or JEDEC Test Standard JS-002	
Latch-Up Test	JESD-78	
Preconditioning Procedure		See Preconditioning Procedure
Pre-HTOL Electrical Test	Per Device Specification	25°C, min., and max. operating temperature
HTOL Test	MIL-STD-883 TM1005	Condition D, T_A = 125°C, 1000 hours min. or T_A = 135°C, 800 hours min.
Post-HTOL Electrical Test	Per Device Specification	25°C, min., and max. operating temperature

5.3 Radiation Related Tests

As a part of one-time, up-front characterization, certain radiation-related tests are performed, as shown in Figure 12.

The radiation levels that a given device is qualified to can be found on its respective datasheet and radiation test reports.

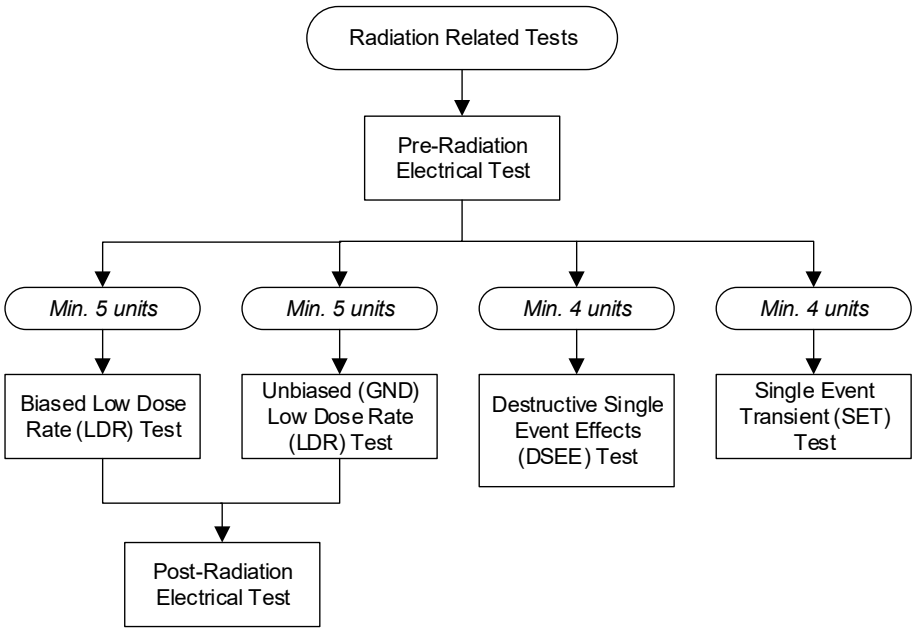

Figure 12. Up-Front Characterization Radiation Related Tests Flowchart

Table 12. Up-Front Characterization Radiation Related Tests

Test	Test Method	Notes
Pre-Radiation Electrical Test	Per device specification, read and record	25°C
Biased Low Dose Rate (LDR) Test	MIL-STD-883 TM1019	Radiation level as per device specification
Unbiased (GND) Low Dose Rate (LDR) Test	MIL-STD-883 TM1019	Radiation level as per device specification
Post-Radiation Electrical Test	Per device specification, read and record	25°C
Destructive Single Event Effects (DSEE) Test	JEDEC Test Standard JESD57A, per device specification	Radiation level as per device specification to assess burnout and latch-up in a heavy ion environment
Single Event Effects (SEE) Test	JEDEC Test Standard JESD57A, per device specification	Radiation level as per device specification

6. Revision History

Revision	Date	Description
1.03	Nov 21, 2024	Updated Table 4.
1.02	Mar 20, 2024	Updated Table 1.
1.01	Jun 23, 2023	Corrected date in the Production Flow section.
1.00	Mar 29, 2023	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.