

Notice To Specification Change HSP48901

TB302 Rev. 1.00 April 1998

Introduction

This is notification of a change to the T_{LCS} Specification of the HSP48901. The new specification is:

		-30 (30MHz)		-20 (20MHz)	
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX
LD Setup Time	T _{LCS}	31	T _{CY} - CLE +2	40	T _{CY} - CLE +2
The Old Specification Was:					
		-30 (30MHz)		-20 (20MHz)	
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX
LD Setup Time	T _{LCS}	28	-	40	-

This parameter specifies the timing for changing the configuration of the part while processing data. This applies mainly to loading coefficients and changing coefficient banks. It does not affect customers who change the part's configuration asynchronously or during periods when no valid data is processed.

This change is being made to achieve a closer match with the specifications for the parts that would be used to generate these signals.

A circuit for implementing this function with the new timing is shown below. The two 74ACT32 gates shown must be in the same package in order to minimize timing skew between them. Using this circuit, the skew will typically be less than 2 nanoseconds over temperature, so that the rising edge of $\overline{\text{LD}}$ will be nearly coincident with the rising edge of CLK, causing $\overline{\text{LD}}$ to take effect during the following clock cycle. By cascading two 74ACT374's, the timing skew with the rest of the system is eliminated; the first synchronizes the output with the local (delayed) clock, while the second synchronizes the output with the rest of the system.

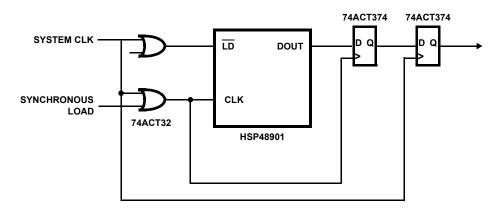


FIGURE 1.

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Renesas Electronics America Inc. 1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A. Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited 9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3 Tel: +1-905-237-2004

Renesas Electronics Europe Limited Dukes Meadow, Milliboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K Tei: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, German Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China Tel: +86-21-2226-0898, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949 Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd. Unit 1207, Block B, Menara Amcorp, Amco Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia

Unit 1207, Block B, Menara Amcorp, Amcorp Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd. No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd. 17F, KAMCO Yangiae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea Tel: +82-2-558-3737, Fax: +82-2-558-5338