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In radio frequency (RF) designs, overcoming spurs is part of the total noise reduction activity. Spurs can add unwanted peaks of energy at frequency offsets where the phase noise is critical for the system to meet error vector magnitude (EVM) goals or output energy masks. For example, in global systems for mobile communications (GSM) applications, having a high-energy spur near an 800 kHz offset from the carrier frequency could be catastrophic for the system by possibly causing it to fail the blocker tests.

This article will look at some of the spurs generated within the phase-locked loop (PLL) device that is used to provide a frequency reference (local oscillator, or LO frequency) to the mixer. The mixer will modulate the baseband or intermediate frequency (IF) signal with the LO frequency to generate a radio signal or an IF signal (or translate the carrier to an IF frequency or a baseband signal in the receive direction). In the process of mixing the two signals in the receive direction, any spurs on the LO frequency reference could result in increased noise on the output around the frequency of interest, thus making it difficult to extract the desired signal. It is critical for the system performance that spurs on the PLL are eliminated, minimized or filtered out before being applied to the mixer.

Spurs in a PLL can be generated by a large variety of sources. Some examples of spur causes are nonlinearities in the PLL building blocks, such as the charge pump, the phase and frequency detector (PFD), and, as is primarily discussed here, the fractional feedback divider operating based on a sigma-delta modulator (SDM). Fortunately, integer boundary spurs are fairly predictable.

## Operation of a Fractional-Feedback PLL

In order to understand the causes and locations of integer boundary spurs, it is necessary to briefly review the circuit functions where these spurs might originate. A fractional-feedback PLL (see Figure 1) makes use of an SDM to generate a voltage-controlled oscillator (VCO) operating frequency ($f_{VCO}$) that is a non-integer multiple of the input reference frequency ($f_{IN}$). This is extremely useful in an RF system that may have to support different carrier frequencies at different times.

**Figure 1. Fractional-Feedback PLL**
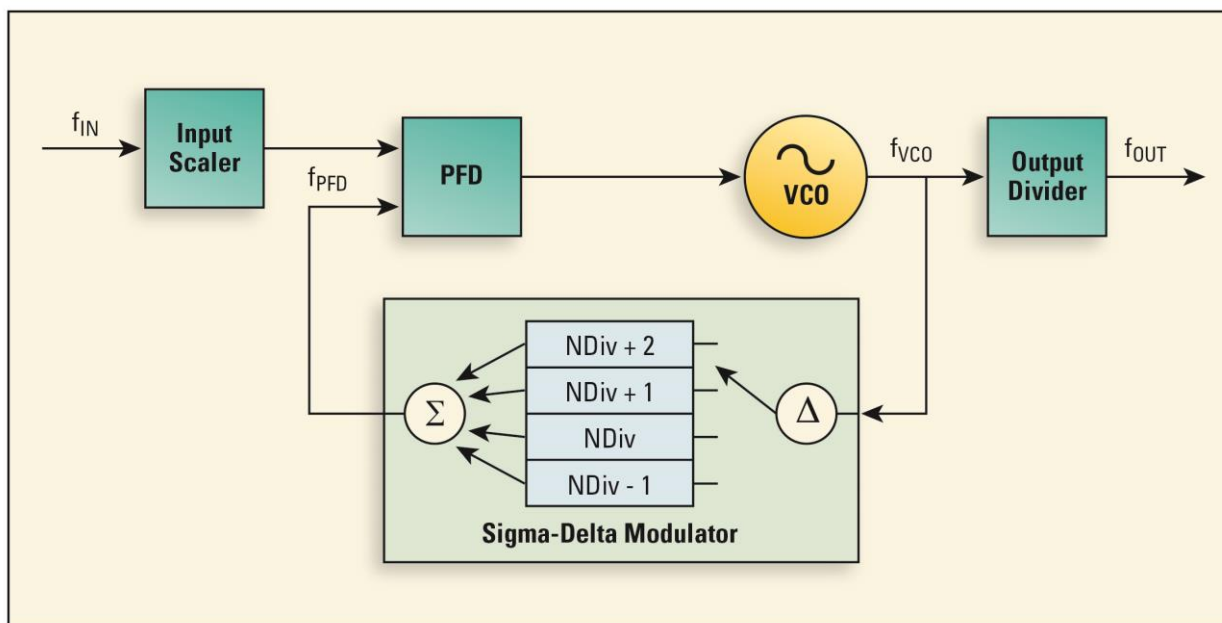
An SDM function has the effect of generating a non-integer divide ratio between the VCO and the PFD in the feedback path of the PLL. The desired non-integer divide ratio consists of an integer portion (NDiv) and a fractional portion (NFrac). For example, if the desired divide ratio is 4.75, NDiv = 4 and NFrac = 0.75. One example of how the SDM achieves this divide ratio is by selecting one of several integer divide ratios slightly above or below NDiv for a period of time. By switching between the available integer dividers, the desired average divide ratio can be achieved as an average over time, even though the instantaneous divide ratio is varying. For example, to achieve an average of 4.75, the SDM could use a divide ratio of 4 for ¼ of the time and a divide ratio of 5 for ¾ of the time. This function will result in spurs as a pattern emerges based on how often each instantaneous division occurs. Actual SDM implementations will use more sophisticated algorithms with, for example, more integer divide ratios, or a modulus function, to attempt to minimize and shape the resulting noise.

## Integer Boundary Spurs—a Special Case of Fractional Spurs

Fractional spurs, including integer boundary spurs, are a common inherent downside of fractional-feedback PLLs. Integer boundary spurs appear when the PLL feedback loop fractional divide ratio is programmed to a value very close to an integer. These spurs occur because the harmonics of the PFD frequency mix with the VCO (or its harmonics) and the resultant intermodulation frequency components fall within the loop bandwidth. This typically occurs when the fractional portion (NFrac) is very small. Some of these spurs are located around the LO fundamental frequency when they pass through the loop bandwidth of the PLL.

Because they fall within the PLL loop bandwidth, they cannot be filtered (by adjusting the order of the loop filter for example) and need to be addressed in a different way. These integer boundary spurs are undesirable because they contribute to the overall integrated RMS jitter, especially spurs located at low frequency offsets below the loop bandwidth. Also, there is a risk of intermodulation between these spurs within the mixer and any adjacent channels, thus increasing the risk for distortion and signal-to-noise ratio impact for the system.

Unintended leakage currents, mismatch between up and down commands, switching transients in the charge pump, quantization noise in the SDM, or even the algorithm used to proceed to a fractional division can be responsible for the generation of spurs.

## Mitigation of Spur Effects

Fractional spurs are just a subset of all the spurs that can be generated inside a PLL, but they are spurs that the system designer can mitigate or predict (and therefore filter or avoid).

As mentioned before, intermodulation between the input reference frequency and the feedback frequency can be responsible for generating a frequency component that modulates the VCO. This causes a fractional spur. Note that the integer boundary spur is generated in a similar way, when the feedback divide ratio is very close to an integer number.

So, in the case of integer boundary conditions—in other words, when the VCO frequency is near an integer multiple of the reference frequency (1.6 GHz + 5 kHz in the example below)—the feedback instantaneous frequency (VCO frequency divided by the instantaneous value of the feedback divider) differs from the reference instantaneous frequency. The PFD will take both inputs and calculate a phase/frequency error. The PFD is not perfect and will have some mixing effects that will create spurs. The closer to an integer multiple of the reference input the VCO frequency is, the more in-band the spur will be located. This occurs because the PFD will mix to a fraction of the feedback frequency or reference frequency. This will create a spur at the fraction frequency.

### Example Demonstrating Boundary Spurs

The following figures illustrate an example of boundary spurs occurring in an application for IDT's 8V97053 High-Performance Wideband Fractional RF Synthesizer/PLL, demonstrating the effect of changing from an integer frequency conversion to a conversion very close to an integer as needed to achieve the target output frequency. In the first case, 1.6 GHz is generated from an integer conversion of a 50 MHz input reference. In the second case, the output is changed to 1.6 GHz plus 5 kHz, which results in boundary spurs due to the fractional divide ratio.

In the first case, 1600 MHz can be generated from 50 MHz by using the input reference doubler with the PFD frequency at 100 MHz as illustrated in Figure 2. Then the PLL multiplies the PFD frequency to a suitable VCO frequency that is within the VCO tuning range. The 8V97051/53 VCO tuning range is 2200 MHz to 4400 MHz. Due to multiplying the PFD frequency by 32, the VCO frequency is 3200 MHz, which is exactly twice the output frequency that needs to be generated (1600 MHz). See Figure 3 for the feedback divider settings. None of these steps includes a fractional divide ratio. Therefore no integer boundary spurs or fractional spurs are observed on the phase noise plot shown in Figure 4.

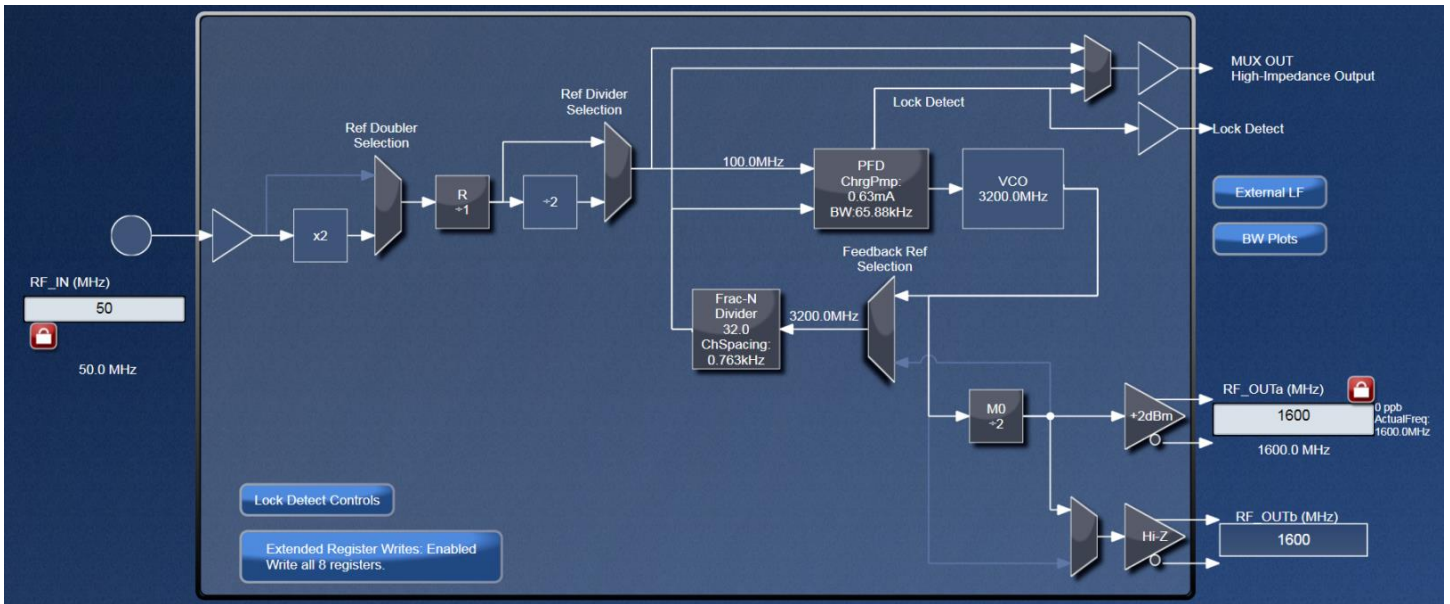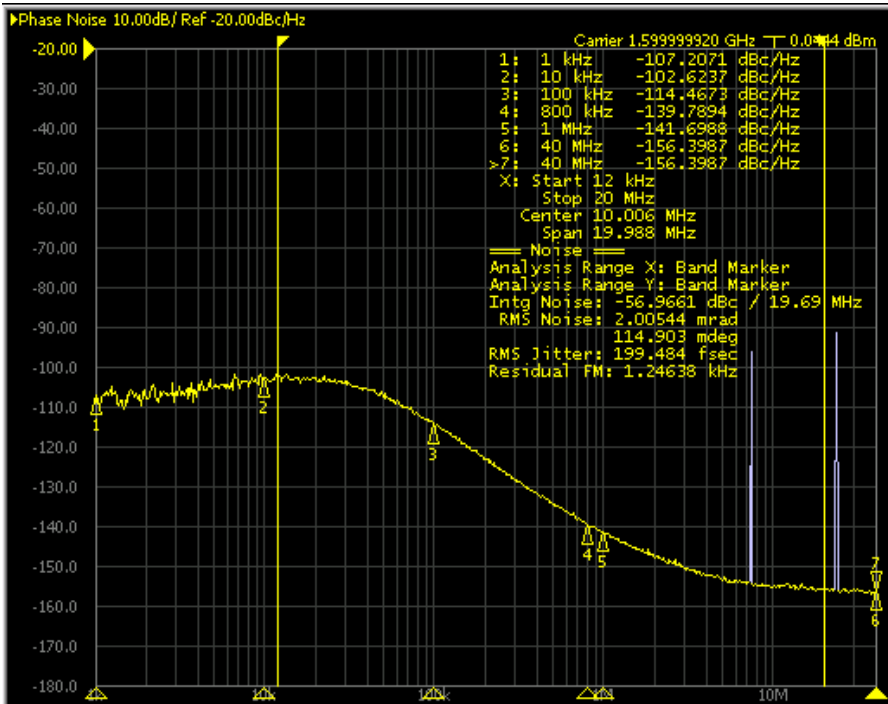**Figure 2.   8V97053 Configuration for 1.6 GHz Output from 50 MHz Input using a 100 MHz PFD Frequency**



**Figure 3.   8V97053 Feedback Divider Settings for 1.6 GHz Output using a 100 MHz PFD Frequency**

**Figure 4.    Phase Noise Plot for 8V97053 Configured to Generate a 1.6 GHz Output from a 50 MHz Input**



In the second case, an output frequency of 1.6 GHz + 5 kHz is desired, so the PLL is forced into a fractional mode. See Figure 5 for the configuration and Figure 6 for the feedback divider settings. The fractional value of the divider is now non-zero and is very small because the additional output frequency step is very small. In this example, using a calculation similar to the first case, the desired feedback divider value is 32.0001, which is very close to the integer value 32.

**Figure 5.    8V97053 Configuration for a 1.6 GHz + 5 kHz Output from a 50 MHz Input with a 100 MHz PFD Frequency**
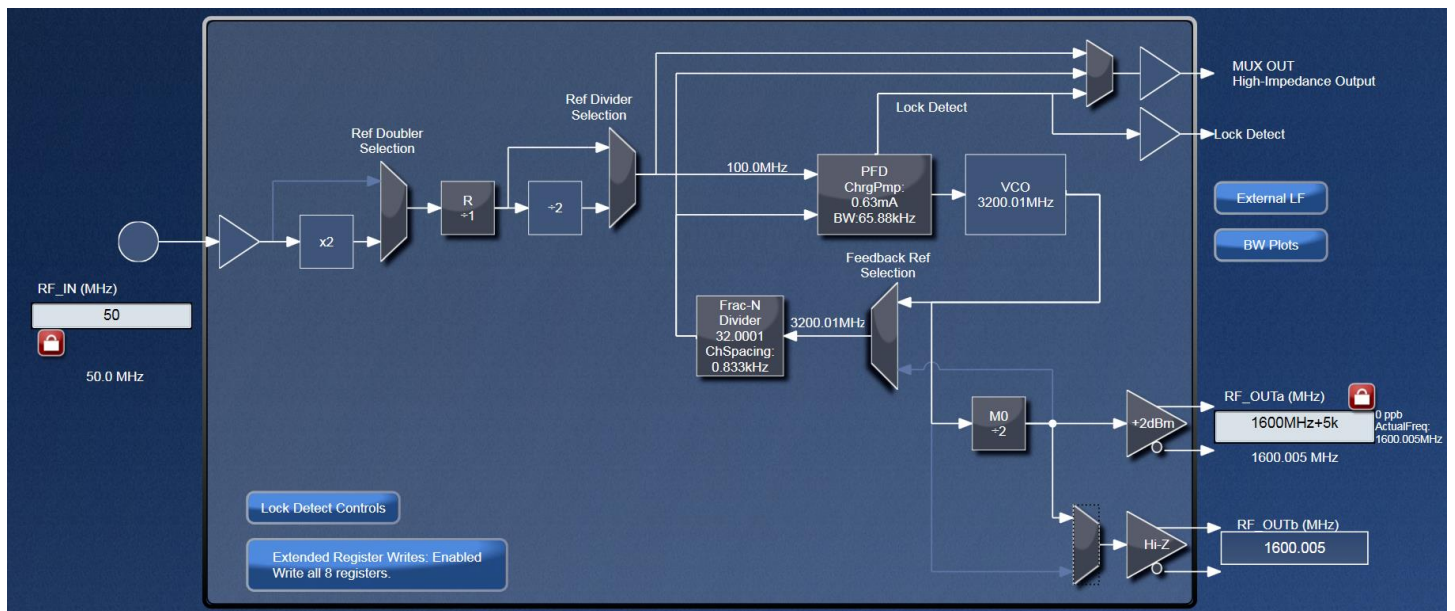
**Figure 6.    8V97053 Feedback Divider Settings for 1.6 GHz + 5 kHz Output with 100 MHz PFD Frequency**



The integer boundary phenomenon is a product of sampling two non-harmonically related frequency components (PFD and VCO for example), which produces a family of spurs that can fall within or near the passband of the loop bandwidth as shown in the phase noise plot in Figure 7. It occurs when the fractional part of the feedback divider is close to 0 or 1. These spurious tones are not attenuated by the loop filter and show up in the spectrum of the RF synthesizer output. As the fractional part of the PLL feedback divider approaches ½ , ¼ , ¾ …, a similar set of the spurs are generated but at lower magnitudes.

**Figure 7.    Phase Noise Plot for 8V97053 Configured to Generate a 1.6 GHz + 5 kHz Output from a 50 MHz Input**
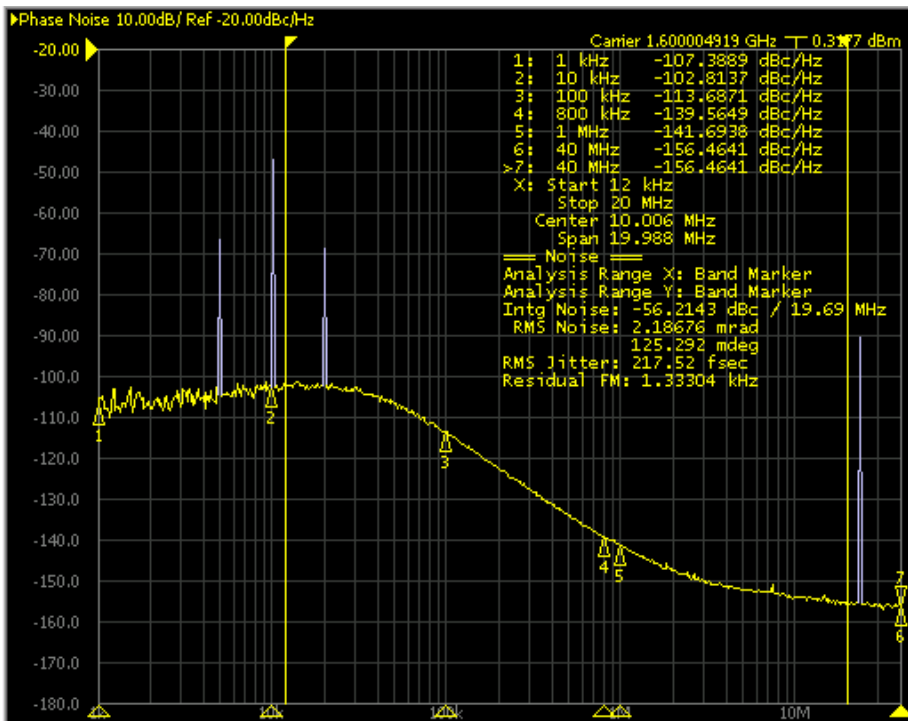
The location of the first-order integer boundary spurs is determined by the difference between the VCO frequency and the nearest harmonic of the reference frequency (or PFD frequency). In the second case example above, that difference is 3200.01 – (100 ∗ 32) = 10 kHz.

More generally, the main integer boundary spur is located at $f_{VCO}$ - ($f_{PFD}$ ∗ NDiv).

$f_{VCO}$ = $f_{PFD}$ ∗ (NDiv + FRAC), where FRAC = FDiv / MOD is the fractional portion of the feedback divider.

As a result, the first order integer boundary spur is located at an offset of $f_{PFD}$ ∗ FRAC.

A second-order (2nd harmonic) integer boundary spur is located at an offset twice that of the first-order integer boundary spur, which is located at 2 ∗ [$f_{VCO}$ - ($f_{PFD}$ ∗ NDiv)]. The second-order integer boundary spur is at 20 kHz in the example above.

In the phase noise plot for the second case, there is also an in-band spur located at half the offset of the first-order integer boundary spur, and sometimes a harmonic related to the output divider can appear (in the second case example above, we use an output divide ratio of 2). That spur is located at 5 kHz in this example. Other spurs could also appear and may be generated by other mechanisms.

Integrated Device Technology (IDT) RF synthesizers and other PLLs implement advanced SDM algorithms to mitigate and reduce these spurs and spread their energy to higher offsets so that their energy is not entirely localized within the loop bandwidth. This is why the 8V9705x products can offer excellent fractional spurs performance. In addition, system designers can mitigate the generation of these near-integer boundary spurs by using a slightly different VCO frequency when possible or by changing the input frequency or the PFD frequency.

Note that in addition to the integer boundary spurs, other spurs may be found at multiples of the PFD frequency and the VCO frequency, and there are in-band spurs that are shaped by the low-pass filter response.

## Other Mechanisms that Cause In-Band Spurs

There are other mechanisms that generate in-band spurs. These can occur when the VCO frequency is coupling with the PFD input frequency or when the VCO frequency is coupling with the [PFD + charge pump] power supply. These are some of the most common cases, but spurs can come from the coupling of almost any block to almost any other block of the PLL, and the coupling can be through layout parasitics, power supplies, bond wires, silicon substrate, sharing of power supplies, etc. When the system designer manages to reduce or eliminate one spur, another one or more could be created.

In addition, square waves (for example, the input reference) are composed of a large number (infinite in theory) of harmonics that are summed together. Some of these harmonics will couple with other internal signals, and the intermodulation products might fall into the PLL bandwidth. These will be present in the in-band section of the phase noise plot, and their power level will be shaped by the loop filter response. Some other reference harmonics will couple in the same way with the VCO signal, but will not be shaped by the PLL loop filter response.

As far as the feedback divider is concerned, a higher order of sigma delta modulation allows spreading the frequency of occurrences for each instant divide value so that the risk for a pattern that can be responsible for creating spurs is decreased. In theory, the fractional-feedback PLL can be free of fractional spurs if the order of the sigma-delta modulation is high enough. A high-order SDM modulates the divider with an uncorrelated control sequence. However, it is not practical to have a too high an order for the sigma delta modulation. Generally, it is accepted that a third-order SDM modulation is a good compromise, practical to implement as well as sufficient to help avoid obvious patterns that could create high energy spurs.

Intermodulation products between the reference frequency and the VCO frequency can also be reduced by providing good supply isolation between the charge pump and the VCO that will reduce noise coupling.

In order to avoid integer boundary spurs, the choice of $f_{IN}$ is important, and when possible, more than one PFD frequency can be used. Also, when possible, using an integer mode for the PLL eliminates the risk of integer boundary spurs.

Integrated Device Technology (IDT) also implements smart algorithms (based on adders and modulus) in the PLL fractional feedback divider's SDM in order to spread the occurrences of instant division values, thus reducing any pattern that could generate high power spurs. The 8V97051, for example, offers multiple choices of algorithm (or SDM types) and a choice of multiple orders of SDM.

For more information on the 8V9705x products, please visit www.idt.com/8v97051.

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